GEORGIA INSTITUTE OF TECHNOLOGY
OFFICE OF CONTRACT ADMINISTRATION
SPONSORED PROJECT INITIATION

Date: April 18, 1979

Project Title: Evaluation and Assembly of X-Band Pulsed GaAs Impatt Diode Chips

Project No: A-2351

Project Director: Mr. Charles T. Rucker

Sponsor: General Dynamics Corporation; Pomona Division; Pomona, CA 91766

Agreement Period: From 2/28/79 Until 9/28/79

Type Agreement: Purchase Order No. P0163130

Amount: $31,9[illegible]3

Reports Required: Monthly Progress Reports; Final Report

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Defense Priority Rating: N/A

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GEORGIA INSTITUTE OF TECHNOLOGY
OFFICE OF CONTRACT ADMINISTRATION

SPONSORED PROJECT TERMINATION

Date: April 4, 1980

Project Title: Evaluation and Assembly of X-Band Pulsed GaAs Impatt Diode Chips

Project No: A-2351

Project Director: Mr. Charles T. Rucker

Sponsor: General Dynamics Corporation; Pomona Division; Pomona, CA 91766

Effective Termination Date: January 18, 1980

Clearance of Accounting Charges: February 18, 1980 for Reporting

Grant/Contract Closeout Actions Remaining:

- [x] Final Invoice and Closing Documents
- [ ] Final Fiscal Report
- [x] Final Report of Inventions
- [x] Govt. Property Inventory & Related Certificate
- [ ] Classified Material Certificate
- [ ] Other _____

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CA-4 (1/79)

A-2351

Monthly Status Letter No. 1

Evaluation and Assembly of X-Band Pulsed GaAs IMPATT Diode Chips

P.O. No. P0163130

Contract period covered
28 February 1979 through 10 April 1979

Submitted to

General Dynamics
Pomona Division
Pomona, California 91766

by

Solid State Sciences Division
Applied Sciences Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting through

Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

Prepared by

C.T. Rucker
W.K. Parks
G.N. Hill

10 April 1979

INTRODUCTION

Although this first Monthly Status Letter is a few days late, we are pleased to report that technical activity is timely and that progress is excellent. Diodes supplied by General Dynamics for this work were not received until March 28, 1979 (1 month after Contract start date). Therefore, this Status Letter reports briefly on work through April 10 rather than March 31, as would normally be the case.

The Solid State Sciences Division of EES is pleased to have the opportunity to assist General Dynamics with this task. We anticipate a successful program.

TECHNICAL STATUS

Phase I calls for detailed evaluation of diode chips, assembly and test of representative individual chips in packages and, if appropriate, fabrication and test of representative unpackaged multichip diodes. The purpose of these tests and experiments is to prove (or disprove) the usefulness of the available chips for multichip work.

Thus far, work has concentrated on assessment of the chips. The preselection process (reference proposal) has been applied to all the device chips and SEM evaluation has begun; capacitance measurements have not started. All of these parameters will be covered in detail, in the second Monthly Status Letter. Preselection data completed to date are summarized in Table 1. Unfilled data positions in this table will be filled as the remaining data are taken. Figure 1 presents the data of Table I in graphical fashion. Although some of these diode chips are defective, an acceptable yield is expected.

DIODE PACKAGING

The diode chips were received in five plastic containers, each containing ten chips. In order to identify the first and tenth chip position in each container, the vendor placed a small square of self adhering label material adjacent to these chips. Unfortunately, these small squares caused sufficient misalignment of the containers to allow the chips to shift throughout the containers so that individual chips could not be identified within the ten chip set. More seriously, many of the chips were found to be tenaciously attached to the adhesive material itself. Removal of these chips from the adhesive cannot be accomplished with solvents because of a gelation effect. Therefore, vacuum pickups and tweezers had to be used. This process is quite hazardous to the chips and some deformation of chip heat sinks was unavoidable. Even so, no fatal damage resulted with any chip.

We recommend the following:

1) That General Dynamics return chips still in their possession (presumably five containers) to Varian for separation, recataloging and retest, if necessary. General Dynamics should check first, of course, to be sure that the problem exists with these chips and

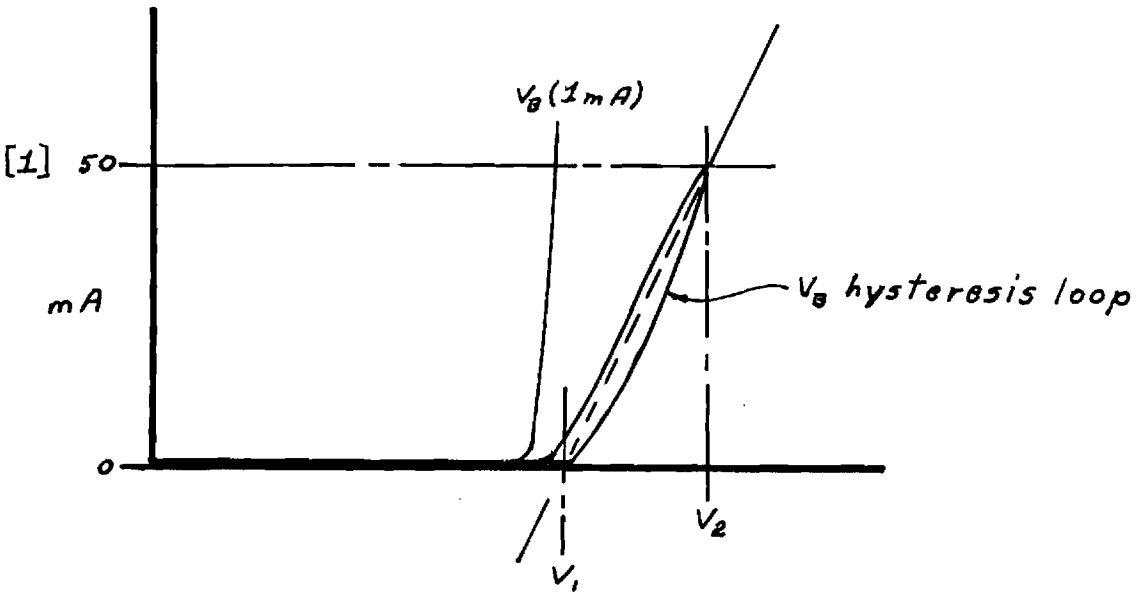
2) That general Dynamics note this problem on any future purchase orders for additional chips.

Unfortunately, this problem prevents us from comparing our data directly with Varian's. Comparisons based on averages within a given container indicate excellent agreement; therefore, we should probably proceed using the chips as planned.

DEFINITION OF PRESELECT PARAMETERS

V_B(1 mA) - the breakdown voltage measured at I = 1 mA. This current is usually sufficient to prevent erroneous V_B readings which sometimes result from premature breakdown and leakage.

V_1 = V_B(intercept) - defined as per sketch below.



PRESELECTION PARAMETERS

V_2 = V_B(50 mA) - the breakdown voltage measured at I = 50 mA. This stress level is usually sufficient to establish the rate of change and change in V_B due to current and associated heating.

F ——— an arbitrary slope parameter defined as the change in V_B (ΔF) normalized to the average of V_2 and V_1. A merit factor of sorts.

DIODE LOT: VSX9251

MANUFACTURER: VARIAN

LOT SUB NO.: E830

PRESELECTION SUMMARY

CHIP NO.	V_B(1mA)	V_1 V(Intercept)	V_2 V_B(50 mA)	ΔV (V_2-V_1)	F $(\frac{2\Delta V}{V_1+V_2})$	$C_j(\approx V_B)$
1	30.0	31.0	35.5	4.5	0.14	
2	28.5	29.5	35.0	5.5	0.17	
3	27.5	28.5	32.5	4.0	0.25	
4	38.5	40.5	49.0	8.9	0.19	
5	35.0	36.0	42.0	6.0	0.15	
6	34.5	36.5	42.0	5.5	0.14	
7	36.0	38.0	47.0	9.0	0.21	
8	37.0	41.0	50.0	9.0	0.20	
9	35.0	36.0	41.0	5.0	0.13	
10	40.0	41.0	49.0	8.0	0.18	
11	39.5	41.5	50.0	8.5	0.19	
12	37.5	38.0	46.0	8.0	0.19	
13	40.0	43.0	55.0	12.0	0.24	
14	34.5	36.0	44.5	8.5	0.21	
15	36.0	37.5	44.5	7.0	0.17	
16	33.5	34.0	39.5	5.5	0.15	
17	33.0	34.0	40.0	6.0	0.16	
18	31.0	37.0	48.0	11.0	0.26	
19	32.0	36.0	43.0	7.0	0.18	
20	29.5	30.5	36.0	5.5	0.17	
21	31.5	33.0	38.5	5.5	0.15	
22	27.5	28.5	33.5	5.0	0.16	
23	30.5	32.0	36.5	4.5	0.13	
24	37.0	38.0	45.5	7.5	0.18	
25	32.0	41.0	52.0	11.0	0.24	
26	*	--	--	--	--	
27	43.5	43.0	51.0	8.0	0.17	
28	38.5	39.0	47.0	8.0	0.19	
29	28.0	29.5	37.0	7.5	0.23	
30	37.0	38.0	46.0	8.0	0.19	

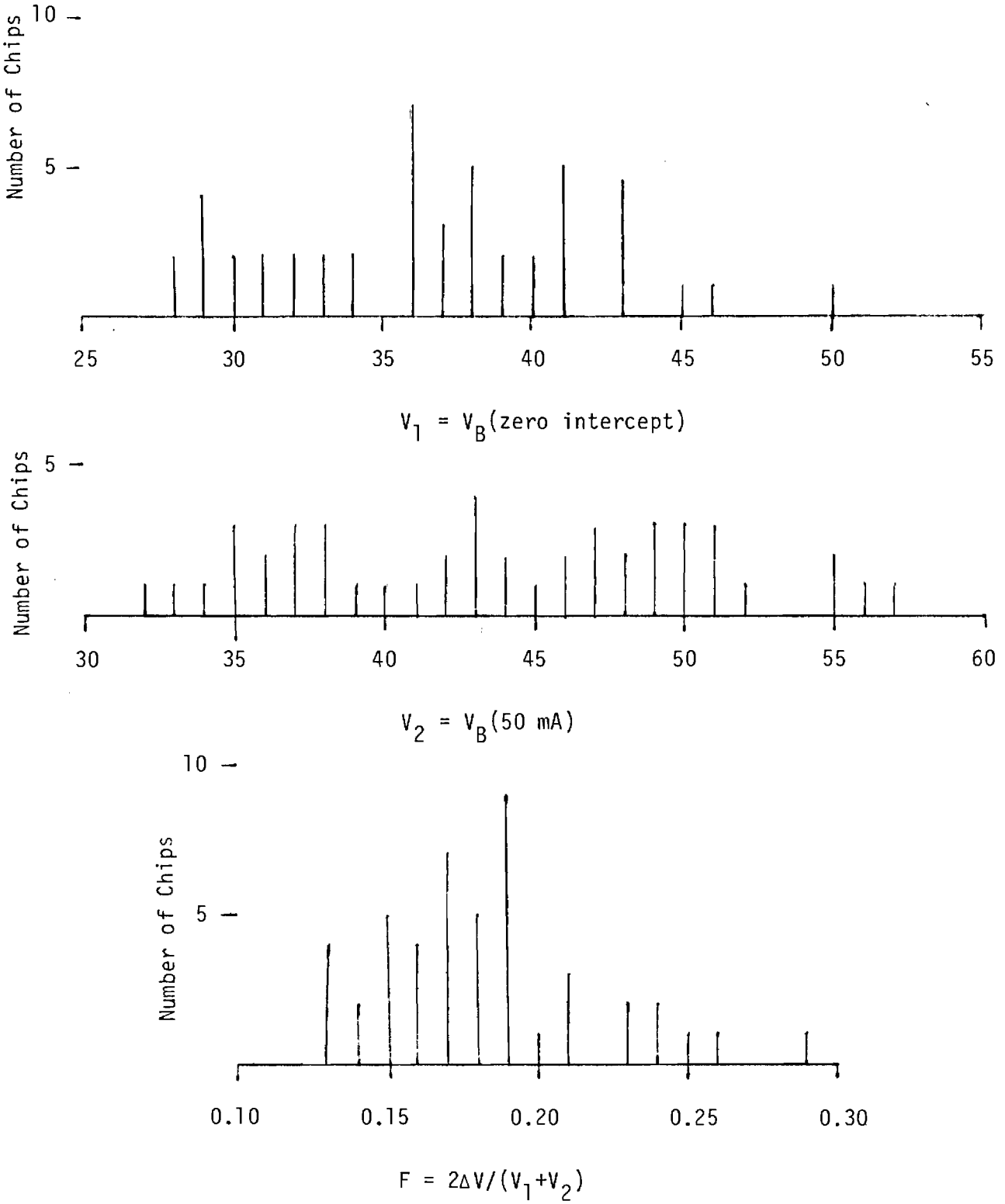


Figure 1. Preselection Data, Graphical Summary

PLANS FOR NEXT MONTH

- Diode chip evaluation will be completed.
- Packaged chips will be assembled and r.f. tested.
- Assembly of the first unpackaged multichip devices will be started.

A-2351

Monthly Status Letter No.2

Evaluation and Assembly of X-Band Pulsed GaAs IMPATT Diode Chips

P.O. No. P0163130

Contract period covered
11 April 1979 through 10 May 1979

Submitted to

General Dynamics
Pomona Division
Pomona, California 91766

by

Solid State Sciences Division
Applied Sciences Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting through

Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

Prepared by

C.T. Rucker
W.K. Parks
G.N. Hill

10 May 1979

GENERAL

This status letter reports progress related to combining X-band pulsed IMPATT diodes supplied by General Dynamics. Work done from April 11 through May 10, 1979 is summarized.

TECHNICAL STATUS

Phase I calls for detailed evaluation of diode chips, assembly and test of representative individual chips in packages, and fabrication of representative unpackaged two-chip diodes. Detailed evaluation of the chips was begun last month, and the preselection process required by the evaluation was completed. This month, capacitance measurements of all fifty diodes were made, and an SEM analysis of selected diodes was also finished. Thus, the initial evaluation of the diodes is complete.

Three single diodes were packaged, and a three-chip diode was also assembled. The three-chip, rather than a two-chip diode, was first fabricated because comparison with similar three-chip diodes from another project is planned. RF testing of the diodes was then begun, but results to date have shown efficiencies and power output for both the single and multichip diodes fall significantly below those recorded by the vendor for "similar" diodes from the same lot. The discrepancy in values may be due to a number of reasons, e.g., the statistically small number of samples for which measurements were made or problems in the Varian instrumentation resulting in optimistic performance. There may also be a problem in the Georgia Tech test setup, and several schemes to examine its accuracy will be pursued during the next report period.

CAPACITANCE MEASUREMENTS

For each diode, #1 - #50, the junction capacitance was measured at a reverse bias of twenty (20.0) volts. These measurements were made after the

completion of the high current preselection test. Although the normal practice at Georgia Tech is to measure the capacitance nearer breakdown, twenty volts was chosen to agree with the measurements made by Varian. The data are presented in the last column of Table 1. The rest of the table contains preselection data reported in the first monthly status letter.

Figure 1 compares the data taken by Varian and Georgia Tech. Because the diode numbering was scrambled during shipping, comparison diode by diode is not possible. However, average values for each box of ten diodes were measured and compared with the Varian average capacitance for the same box. The Georgia Tech measurement of capacitance was lower than that of Varian. The discrepancy is probably due either to an instrumentation or an operator variable.

SEM ANALYSIS

From the preselection data, a total of fifteen diodes were chosen for SEM analysis. Five were chosen because they exhibited good V-I curves; ten were chosen due to various abnormalities appearing in their V-I curves.

Figure 2 is representative of a diode with a good V-I curve (#1). Note the excellent geometry of the mesa. The point on the mesa near left center is typical of the Varian etch process, but is not known to affect the diode's performance. The metallization on the back contact appears to be thinner than normal. Thin metallization is much more apparent in the diode of Figure 3. This diode exhibited extreme "walkout", as can be seen in the data of Table 1 (i.e., V_B(1 ma) = 22.5v, while V_B(50 ma) = 56.0v). The poor contact metallization could result in heating of the back contact which in turn could cause heating of the diode junction. We do not plan to dwell upon this problem unless it causes unacceptable problems in the multichip diodes.

Figure 4 is a view of a diode (#19) which had premature breakdown at low current. The deviation from circular mesa geometry is due to improper etching, but has not been known to contribute to premature breakdown in the past. However, the geometric defects at the mesa-heat sink interface, like the one in the photo near the center of the interface, are often associated with contamination. Contamination is often the cause of premature breakdown.

A more graphic example of geometric irregularities at the heat sink-mesa interface is presented in Figure 5. Diode #26 failed during the high current preselection test, and the photo shows that the burnout is at the site of the defect.

For the other diodes analyzed, these observations were strengthened. Diodes with good V-I curves had regular geometries. Problems such as excessive walkout, premature breakdown, or high current failure could be traced to defects such as poor back contact metallizatiom, possible contamination of the heat sink-mesa interface, or excessive overhang of the back contact metallization.

RF TESTING

Three single diodes were mounted in packages. Diode #2 was mounted in an N-33 package and redesignated VSX9251AM-A. Diodes #1 and #3 were mounted in N-57 packages and redesignated VSX9251AM-B and VSX9251AM-C, respectively. A three-chip assembly consisting of diodes #6, #16, and #47 was fabricated and designated VSX9251AM-D.

For the three packaged diodes, a moderate attempt at RF optimization was made, then the following data were taken:

VSX9251AM-A (#2)

(v)	(A)	(W)	(W)	(%)	(GHz)	(μsec)	(%)
V	I	P	Po	η	fo	P.W.	Duty
51.0	1.20	61.2	9.12	14.9	9.2	1	20

VSX9251AM-A (#2)

V	I	P	Po	η	fo	P.W.	Duty
52.1	1.52	79.2	12.9	16.2	10.4	1	20

Diode failed when it dropped mode.

VSX9251AM-C (#3)

V	I	P	Po	η	fo	P.W.	Duty
45.0	1.55	69.8	9.54	13.7	10.5	1	20

The data show an average power output of 10.5 watts per chip and an average efficiency of 14.9% for the three diodes, a poor showing by comparison with vendor data on packaged diodes, Varian S/N VSX9251AM, 1-10.

Of the remaining diodes, three were chosen whose voltage breakdowns and capacitance closely matched. These were used to fabricate VSX9251AM-D; see Figure 6 for an SEM photo of the assembly. Again, the test fixture was adjusted for maximum power, and the data below were taken:

VSX9251AM-D

Three-Chip Assembly (#6, #16, #47)

V	I	P	Po	η	fo	P.W.	Duty
146	1.6	234	33.5	14.3	10.2	1	20

The whole assembly ran at 14.3% efficiency with an average of 11.2 watts output from each diode in the assembly. It should be noted that the data taken for the single and multichip assemblies are self-consistent. The single diodes all averaged outputs of ~ 11 watts at ~ 15% efficiency; the multichip output was 3 x 11 = 33 watts at ~15% efficiency.

In assessing the data from initial RF testing, the low efficiencies for both single and multichip diodes are disturbing when compared with efficiencies of ~25% measured by the vendor on the same lot. The possibility exists that there is a problem with the Georgia Tech test setup. The test fixture was taken apart and cleaned, then the scope recalibrated against an external reference; but neither of these procedures affected the efficiency measurement significantly. A multichip assembly built for another sponsor was put into the setup and gave the same results as recorded several months prior—indicating that nothing in the setup has developed problems recently.

In an attempt to explain the discrepancy, three further actions will be pursued:

1) Complete recalibration of the test system.

2) Use a top hat test fixture. The test fixture presently in use is a Kurokawa type with interchangeable transformers. It can be converted to a top hat type, which in some cases, results in improved diode performance.

3) Comparison with diodes measured by Varian. Ten diodes were mounted in N-57 packages and evaluated by Varian to give an average 18.2 watts output at 25.6% efficiency. These diodes have been requested by C. T. Rucker of Georgia Tech from C. Mason of General Dynamics. Comparison of the two sets of diodes should show whether or not the diodes supplied Georgia Tech are actually lower in efficiency than those packaged by Varian, or whether there exists a problem in the measurements taken by Varian and/or Tech.

PLANS FOR NEXT MONTH

In the next report period, the test setup will be examined and recalibrated as explained in the previous section. Also two or three two-chip assemblies will be fabricated and RF tested in accordance with the requirements of Phase I of the proposal. Once the two-chip assemblies are tested, Phase I of the project will be completed, and work on Phase II can proceed.

DIODE LOT: VSX9251

MANUFACTURER: VARIAN

LOT SUB NO.: E830

PRESELECTION SUMMARY

CHIP NO.	V_B(1mA)	V_1 V(Intercept)	V_2 V_B(50 mA)	ΔV (V_2-V_1)	F $(\frac{2\Delta V}{V_1+V_2})$	$C_j(\simeq V_B)$
1	30.0	31.0	35.5	4.5	0.14	**
2	28.5	29.5	35.0	5.5	0.17	**
3	27.5	28.5	32.5	4.0	0.25	4.82
4	38.5	40.5	49.0	8.9	0.19	3.78
5	35.0	36.0	42.0	6.0	0.15	4.71
6	34.5	36.5	42.0	5.5	0.14	4.08
7	36.0	38.0	47.0	9.0	0.21	4.33
8	37.0	41.0	50.0	9.0	0.20	4.45
9	35.0	36.0	41.0	5.0	0.13	4.12
10	40.0	41.0	49.0	8.0	0.18	4.37
11	39.5	41.5	50.0	8.5	0.19	3.66
12	37.5	38.0	46.0	8.0	0.19	4.57
13	40.0	43.0	55.0	12.0	0.24	3.58
14	34.5	36.0	44.5	8.5	0.21	3.65
15	36.0	37.5	44.5	7.0	0.17	4.48
16	33.5	34.0	39.5	5.5	0.15	4.53
17	33.0	34.0	40.0	6.0	0.16	3.89
18	31.0	37.0	48.0	11.0	0.26	4.65
19	32.0	36.0	43.0	7.0	0.18	4.32
20	29.5	30.5	36.0	5.5	0.17	5.06
21	31.5	33.0	38.5	5.5	0.15	4.97
22	27.5	28.5	33.5	5.0	0.16	5.40
23	30.5	32.0	36.5	4.5	0.13	4.81
24	37.0	38.0	45.5	7.5	0.18	4.03
25	32.0	41.0	52.0	11.0	0.24	3.57
26	*	--	--	--	--	--
27	43.5	43.0	51.0	8.0	0.17	3.89
28	38.5	39.0	47.0	8.0	0.19	4.37
29	28.0	29.5	37.0	7.5	0.23	4.69
30	37.0	38.0	46.0	8.0	0.19	4.21

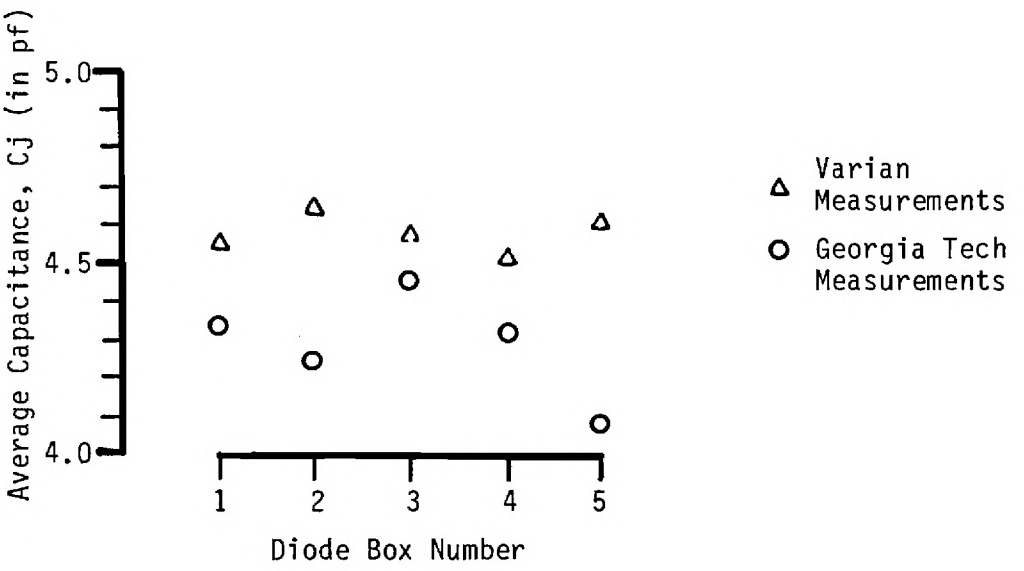


Figure 1. Comparison of Capacitance Measurements, Cj (20v), Taken by Varian and Georgia Tech.

Figure 2. Chip (VSX9251AM, #1) Mag. = 143x. Typical Diode Showing Excellent Nominal Geometry.

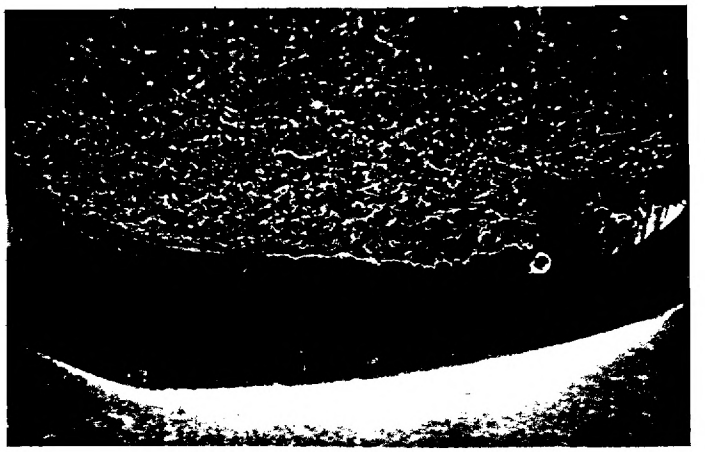


Figure 3. Chip (VSX9251AM, #41) Diode With Excessive Walkout Showing Poor Back Contact Metalalization. Mag. = 357x.

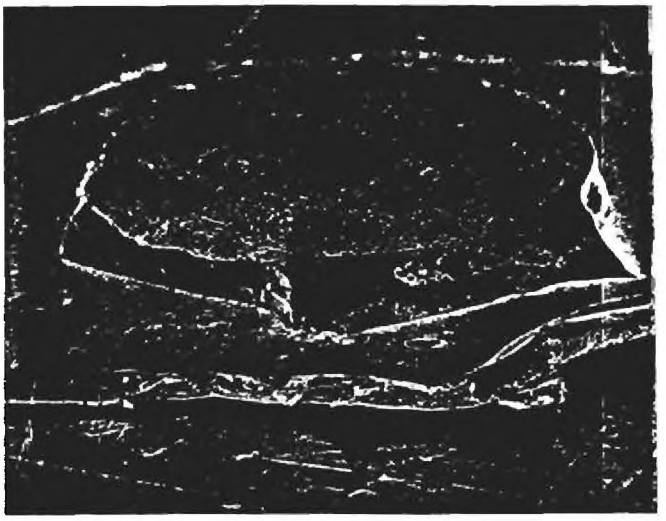


Figure 4. Chip (VSX9251AM, #19) Mag. = 238x. Diode With Non-circular Mesa Geometry.

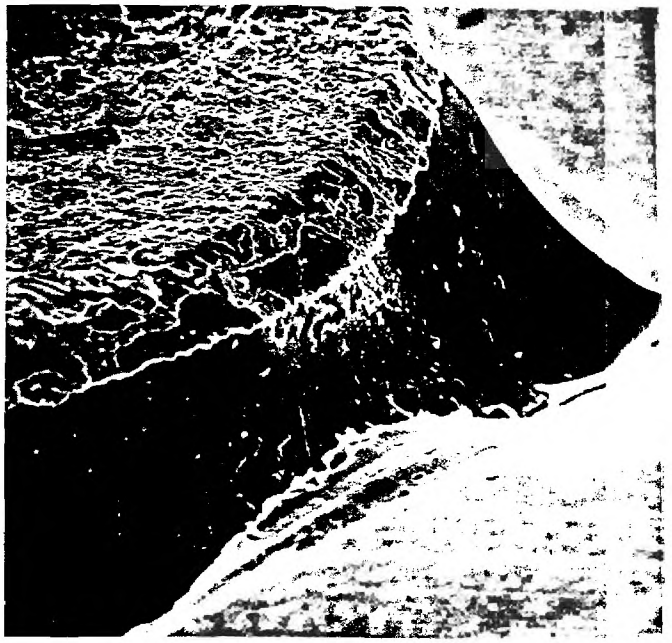


Figure 5. Chip (VSX9251AM, #26) Mag. = 238x. Failed Diode Showing Geometrical Defect at Mesa-Sink Interface.

Figure 6. Assembly (VSX9251AM-D) Mag. = 30x. Three Chip Assembly.

Monthly Status Letter No. 3

Evaluation and Assembly of X-Band Pulsed GaAs IMPATT Diode Chips

P.O. No. PO163130

Contract period covered
11 May 1979 through 10 June 1979

Submitted to

General Dynamics
Pomona Division
Pomona, California 91766

by

Solid State Sciences Division
Applied Sciences Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting through

Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

Prepared by

C.T. Rucker
W.K. Parks

14 June 1979

INTRODUCTION

This status letter reports progress in the series connection of X-band IMPATT diodes (lot No. VSX9251AM). Work done from May 11 through June 10, 1979 is summarized. During the report period, calibration of the system was checked and several two-chip unpackaged diodes were fabricated. Also included with this letter as an appendix is a set of sketches describing the test fixture in use with the two-chip unpackaged assemblies.

SYSTEM CALIBRATION

During the second report period, several diodes were packaged and r.f. tested. The power output and efficiency measurements made on these diodes did not agree with those recorded by the manufacturer on different diodes from the same lot. In particular, the power output averaged about 10.5 watts and the efficiencies were less than 15%, as compared to vendor data of about 18 watts output at 25.6% efficiency.

In order to further investigate this problem, several procedures were effected. First, the original test setup was recalibrated and data was taken on a single packaged diode designated VSX9251AM-A:

(v)	(A)	(W)	(W)	(%)	(GHz)	(μsec)	(%)
V	I	P	P_o	η	f_o	P.W.	Duty
53.0	1.50	79.5	9.12	11.5	9.2	1	20

The test fixture was then converted from a Kurokawa type with coaxial transformer to a top hat type fixture. The latter fixture does not have a matching transformer directly at the diode mount; instead, it has a top hat at the tip of the center conductor to help match the diode to the external circuit. From the top hat setup, slightly less power (P_o = 8.12 watts (at approximately the same efficiency (η = 11.3%) was obtained.

The test fixture was then returned to the Kurokawa configuration. Next, an alternate test setup, using waveguide instead of coax, between the fixture the the power meter was installed. After calibration of the system, the same diode was again tested and showed lower power (P_o = 8.30 watts) at slightly higher efficiency (η = 12.0%) than the original measurement. Also, in the waveguide system, a measurement was made on another single packaged diode (VSX9251AM-C) which closely agreed with the initial measurement taken on the same diode in the original coaxial setup.

Based on this examination of the test setups and calibrations, the cause of the discrepancy between the Varian and Georgia Tech measurements of the r.f. performance of the diode was not apparent. No further investigation is anticipated until the diodes packaged and measured by Varian become available. We are awaiting further word from General Dynamics regarding these diodes

UNPACKAGED TWO-CHIP ASSEMBLIES

As mentioned in Monthly Status Letter No. 2, Phase I of the task will be completed when representative unpackaged diodes are fabricated and supplied. Three two-chip diodes were fabricated this month, however, the r.f. test of only one diode of the three was completed satisfactorily.

Diode assembly VSX9251AM-E was the first built. During the initial stages of r.f. testing, the diamond chip used as a base upon which the diodes are mounted lifted off the puck at low current (~0.6 amp). This problem was cleared up on the next assembly by an additional step in the cleanup procedure prior to bonding the diamond to the puck. The second assembly, VSX9251AM-F (chips #29 and #35), was then tested with the following results.

V	I	P	P_o	η	f_o	P.W.	Duty
104.0	1.52	158	15.1	9.6	10.0	1	20

The assembly was then placed in the top hat fixture and with appropriate tuning higher power and efficiency measurements were obtained:

V	I	P	P_o	η	f_o	P.W.	Duty
98.0	1.50	147	19.7	13.4	11.1	1	20

The test fixture was then reconverted to the Kurokawa configuration for one last measurement, but the top diode of the assembly failed at a power level below that previously obtained.

The third assembly, VSX9251AM-G (chips #37 and #48), failed due to a coolant leak within the test fixture. Because none of the three diodes is presently in operating condition, two more unpackaged two-chip assemblies will be fabricated, tested, and supplied to General Dynamics in order to bring Phase I to completion.

TEST FIXTURE

Attached as an appendix to this letter is a set of drawings outlining the test fixture in use with two chip diode assemblies. No detailed shop assembly drawings were made; only working sketches sufficient for Georgia Tech shop personnel to machine one fixture. The eleven drawings included in the appendix are:

(1) P.N. X3417-1: Test Fixture

(2) P.N. X3417-2: Transformer

(3) P.N. X3417-3: Cooling Head

(4) P.N. X3417-4: Center Conductor

(5) P.N. X3417-5: Center Conductor Extension

(6) P.N. X3417-6: Insert

(7) P.N. X3417-7: Ferrule

(8) P.N. X3417-8: Bias Ferrule

(9) Materials List

(10) Exploded View of Center Conductor Assembly

(11) Side view of Test Fixture with Diode Matching and Cooling Assemblies Installed.

The transformer (P.N. X3417-2) shown is the explicit transformer used for two-chip tests. Other diodes or geometries can be accomodated by changing the dimensions of the transformer. The fixture is designed to accept interchangeable transformers, so that additional transformers may be machined and used during testing. However, if the transformer length is altered significantly, the length of the insert (P.N. X3417-6) may also have to be changed so that the cooling head can make a proper seal against the insert.

The bias ferrule (P.N. X3417-8) fits the center conductor extension (P.N. X3417-5) and its position is adjusted to obtain the highest power output and efficiency. In the exploded view diagram, a spring is shown which fits over the .120" diameter rod of the center conductor (P.N. X3417-4). The spring was chosen to give 35 to 40 grams pressure on the diode, and also to fit in the .189" diameter counterbore of the nylon ferrule (P.N. X3417-7). No further specifications are available on this spring.

The test fixture is designed so that an adjustable short circuit is attached to one side, and a slide screw tuner to the other.

PLANS FOR NEXT MONTH

° Fabricate, r.f. test and supply two unpackaged two-chip assemblies to General Dynamics.

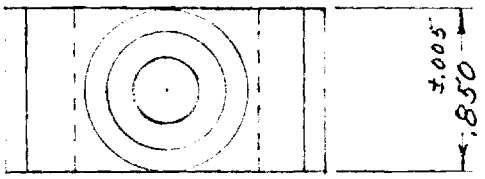
° Proceed with Phase II.

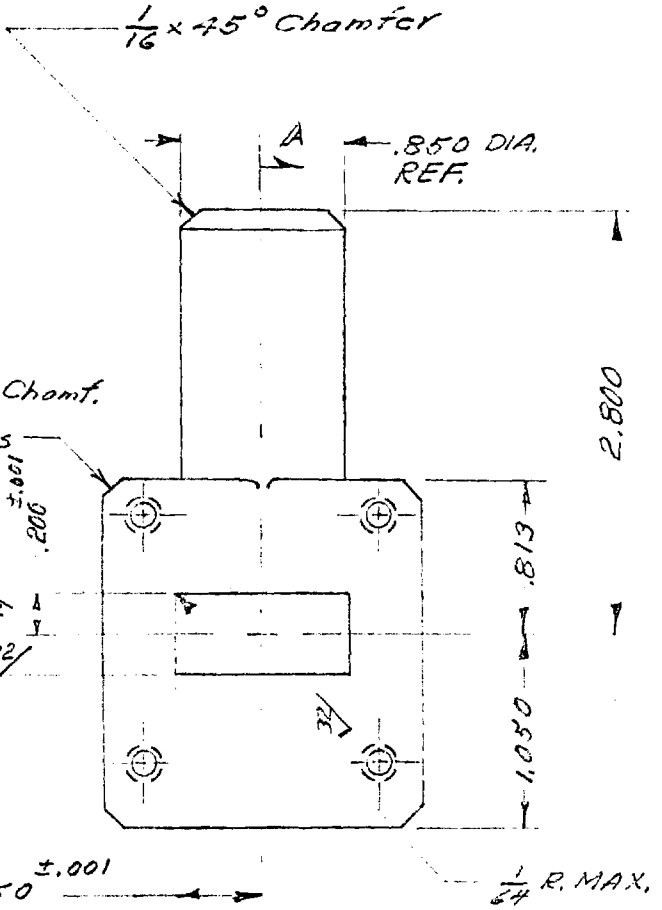
APPENDIX

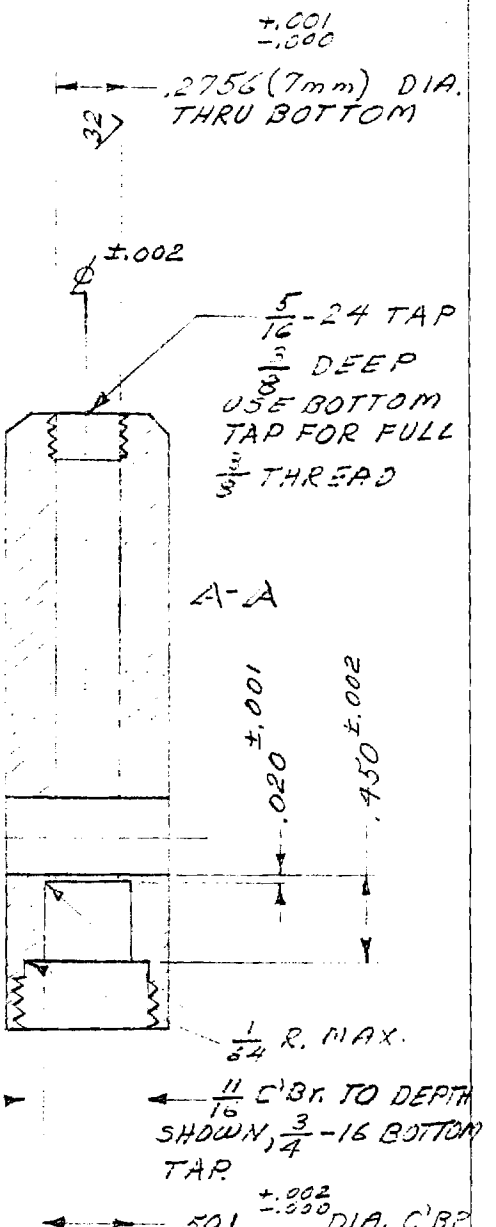
Test Fixture Sketches

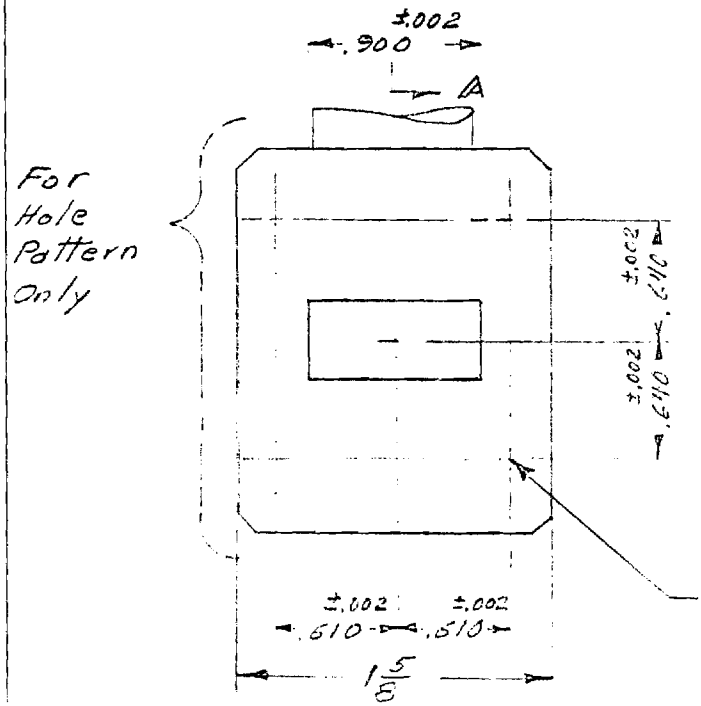
TEST FIXTURE	X-BAND	C. T. Rucker (3417)	3/5/7

P.N. X3417-1







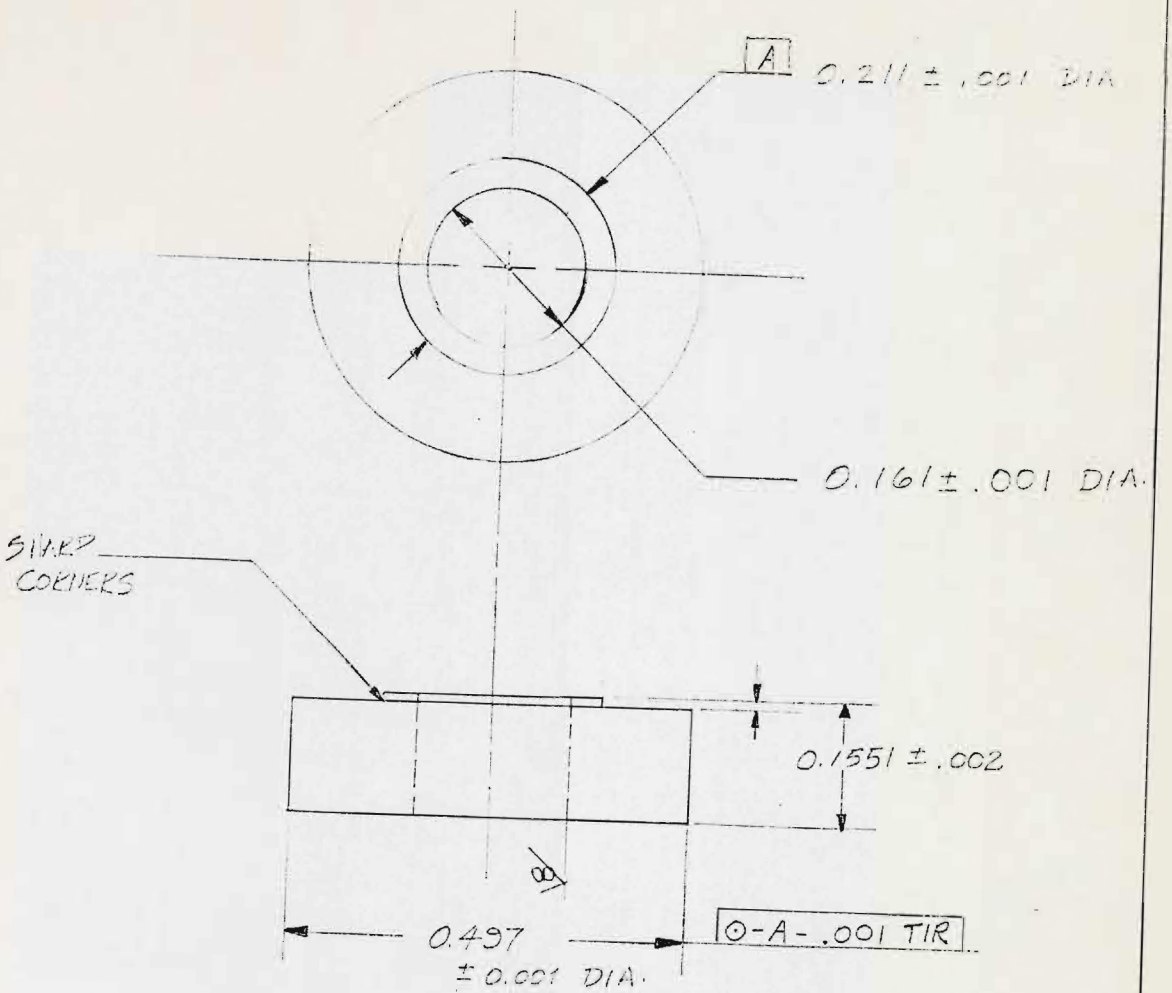


NOTE: SOME DOTTED LINES OMITTED FOR CLARITY.

MATL.: ALUMINUM
≈ 1 x 3 1/2 x 1 3/4

Scale: ≈ 1:1

P.N. X3417-2



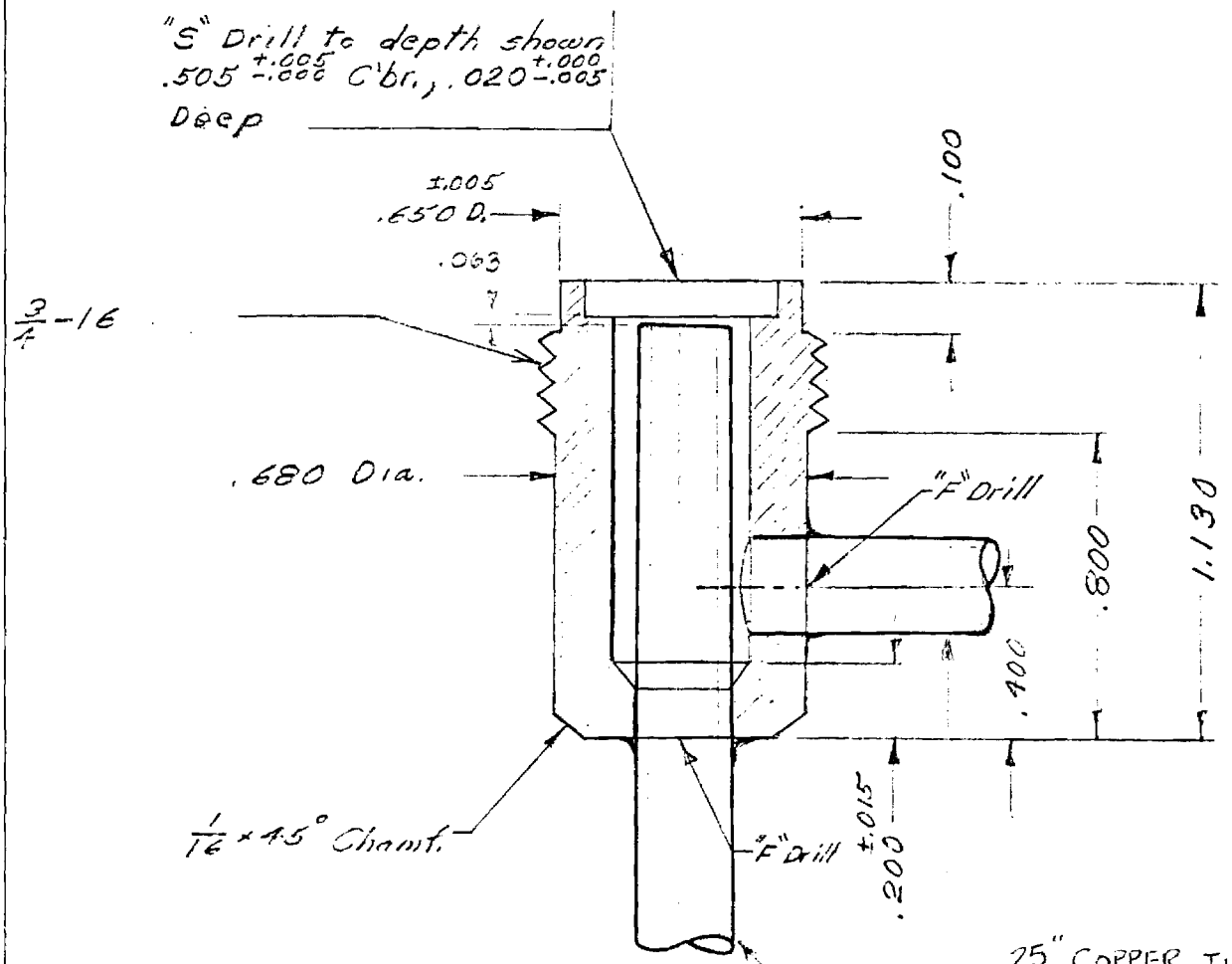
NO SCALE

MATERIAL : COPPER

NOTE: COMPLETED PART FITS .501 HOLE OF P.N. X3417-1

HEAD	X-BAND	C.T. Rocker (3417)	3/5/47

P.N. X3417-3



Scale: ≈ 2:1

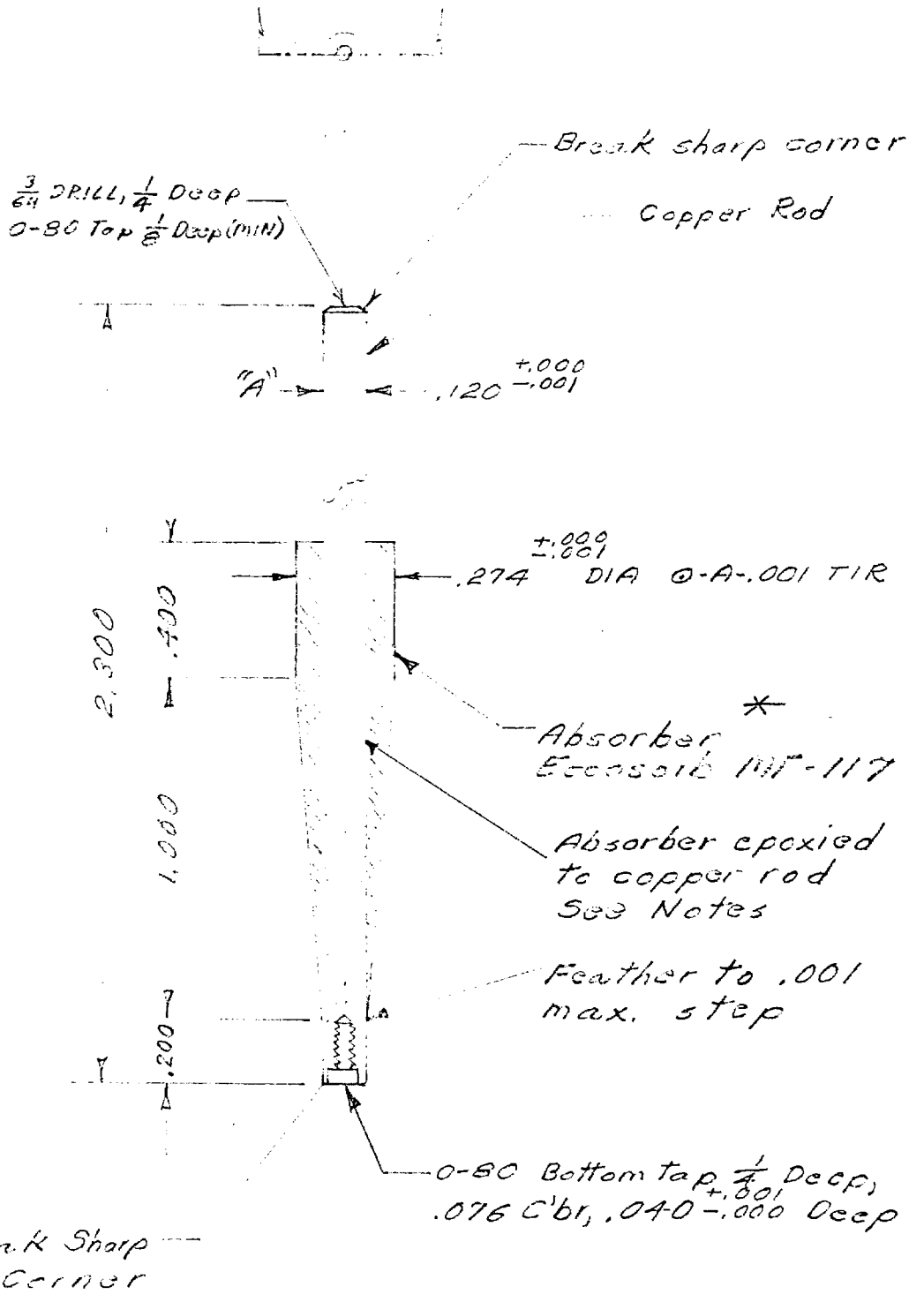
Matl: Yellow brass

Note: Completed part fits P.N. X3417-1

CENTER COND	X-BAND	C.T. Rucker (3417)	3/6/72

R.N. X3417-4

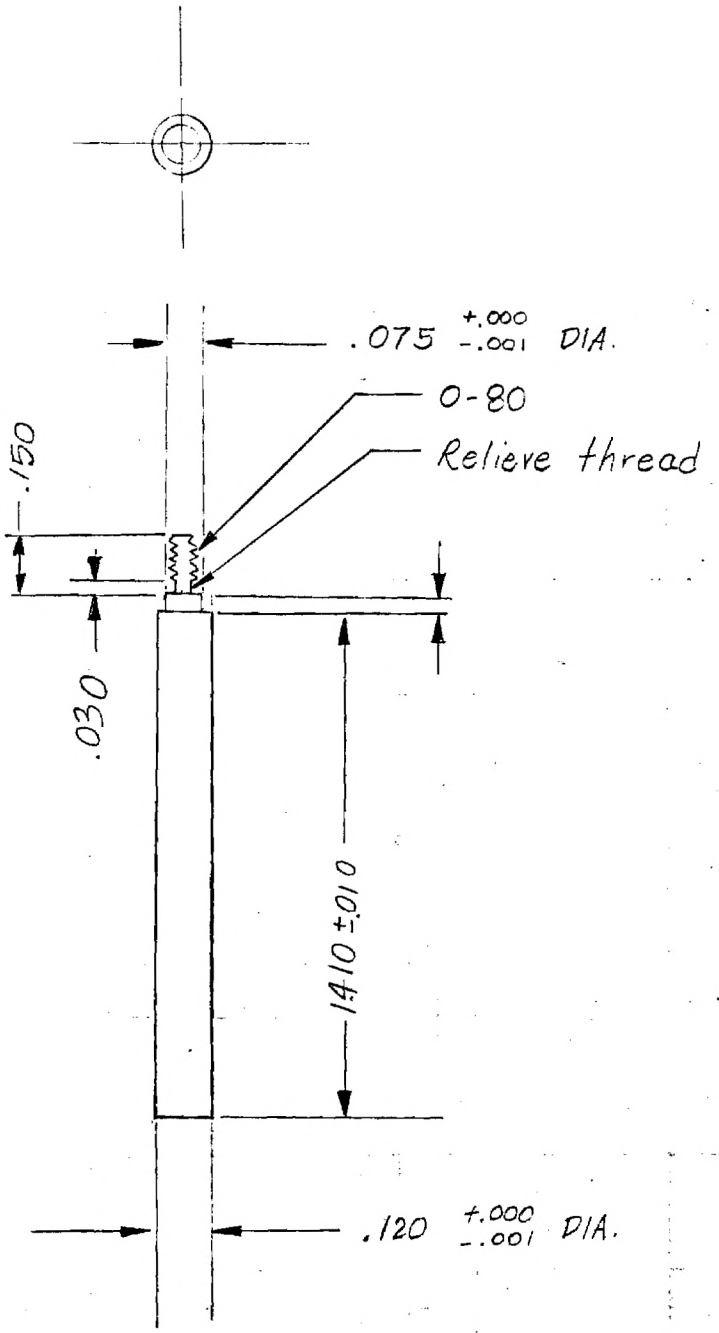
Notes: 1. Machine rod
2. Rough machine absorber
3. Epoxy absorber to rod
4. Final machine including taper
5. Completed part fits .2255 hole per D.W. X3417-1



* Oulls steel tools - use tungsten carbide when possible.
Eccosorb mfg. by Emerson/Cummings

EXTENSION	X-BAND	W. K. PARKS	6/6/13

P.N. X3417-5

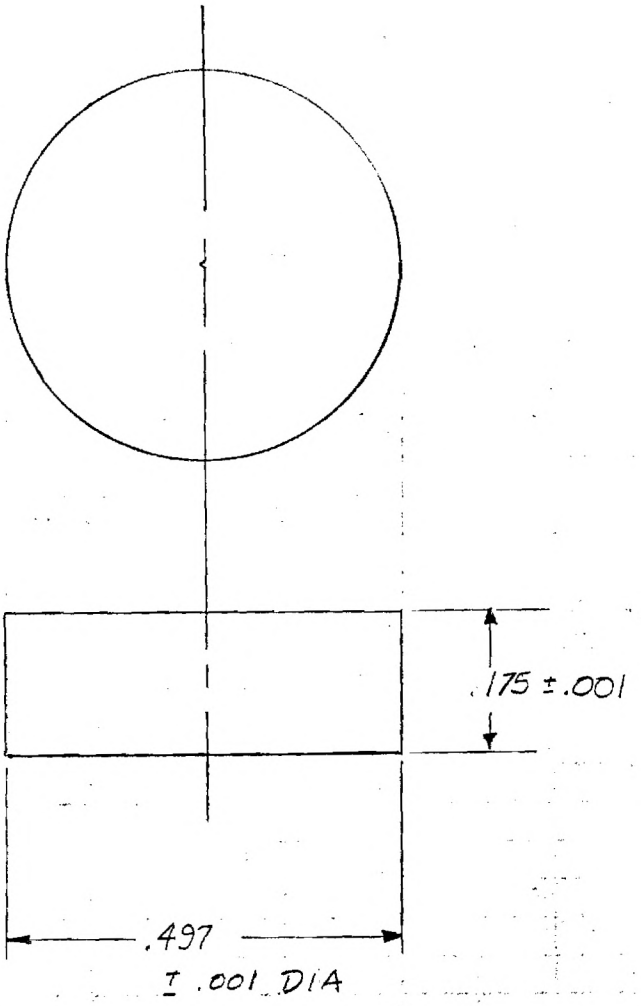


MATERIAL : COPPER

NOTE : COMPLETED PART FITS P.N. X3714-4

INSERT	X-BAND	W.K. PARKS 6/4/79

P.N. X3417-6

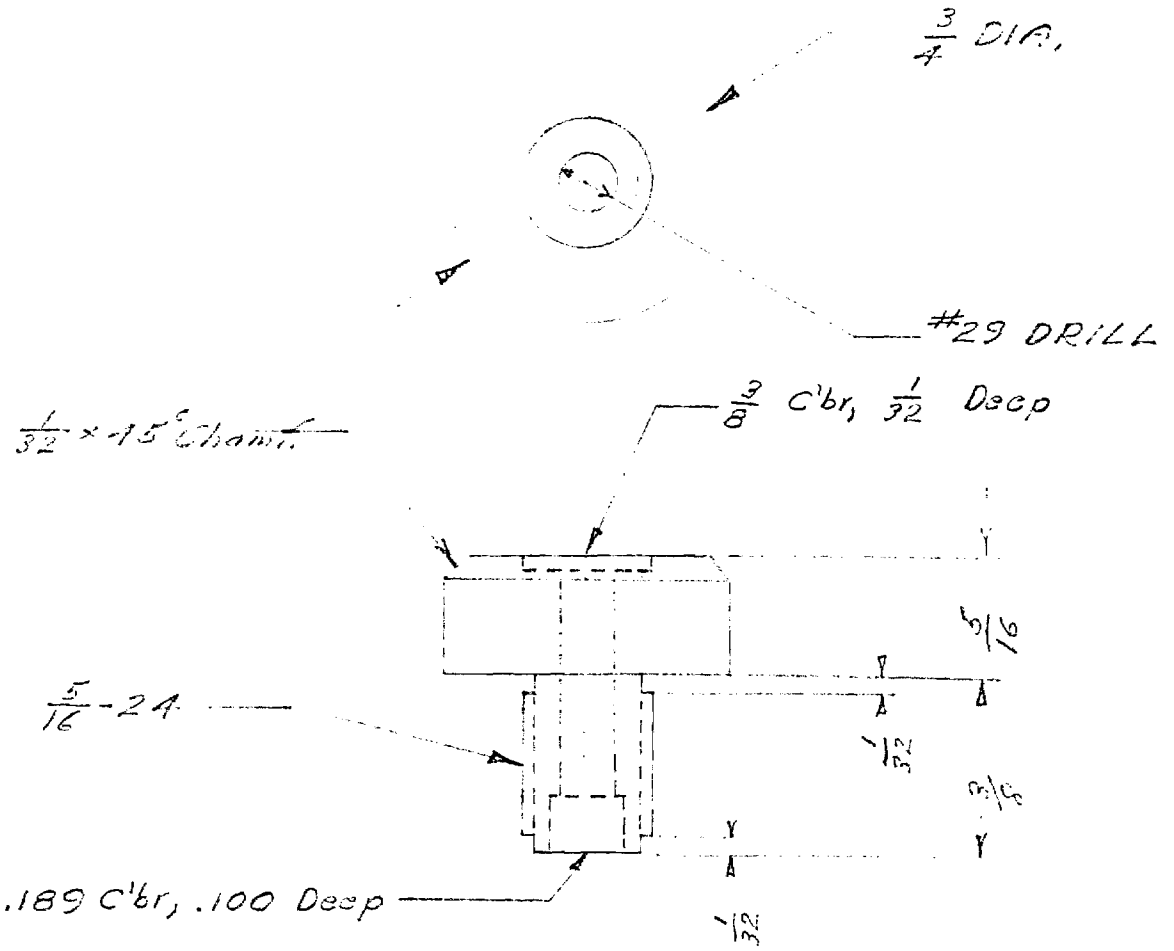


SCALE: ≈ 4:1

MATERIAL: COPPER

FEP2003	X-BAND	C. T. Rucker (3417) 3/6/17

P.N. X3417-7

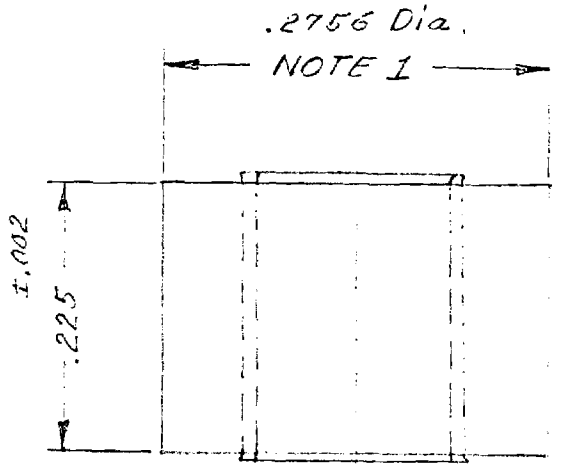


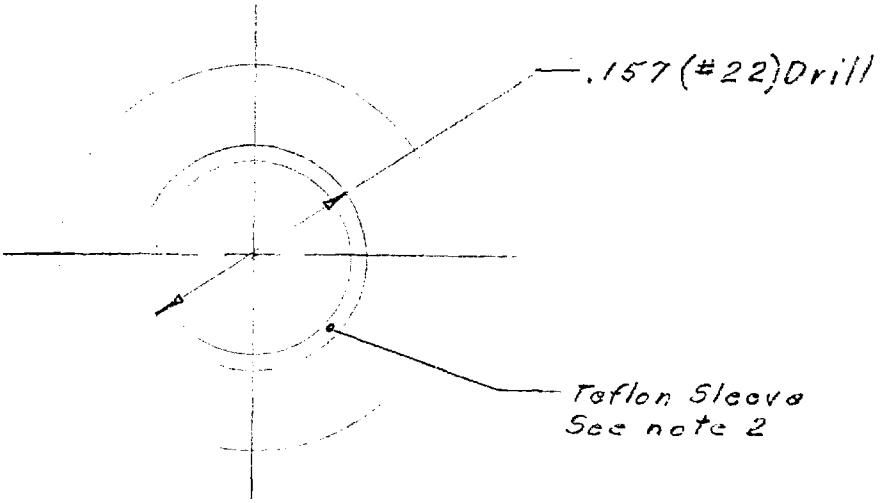
NOTE: PART FITS X3417-1 (5/16-24 hole)

MAT'L.: Nylon

BIAS FERRULE	X-BAND	C.T. Rucker (3/11/71)	3417

P.N. X3417-8





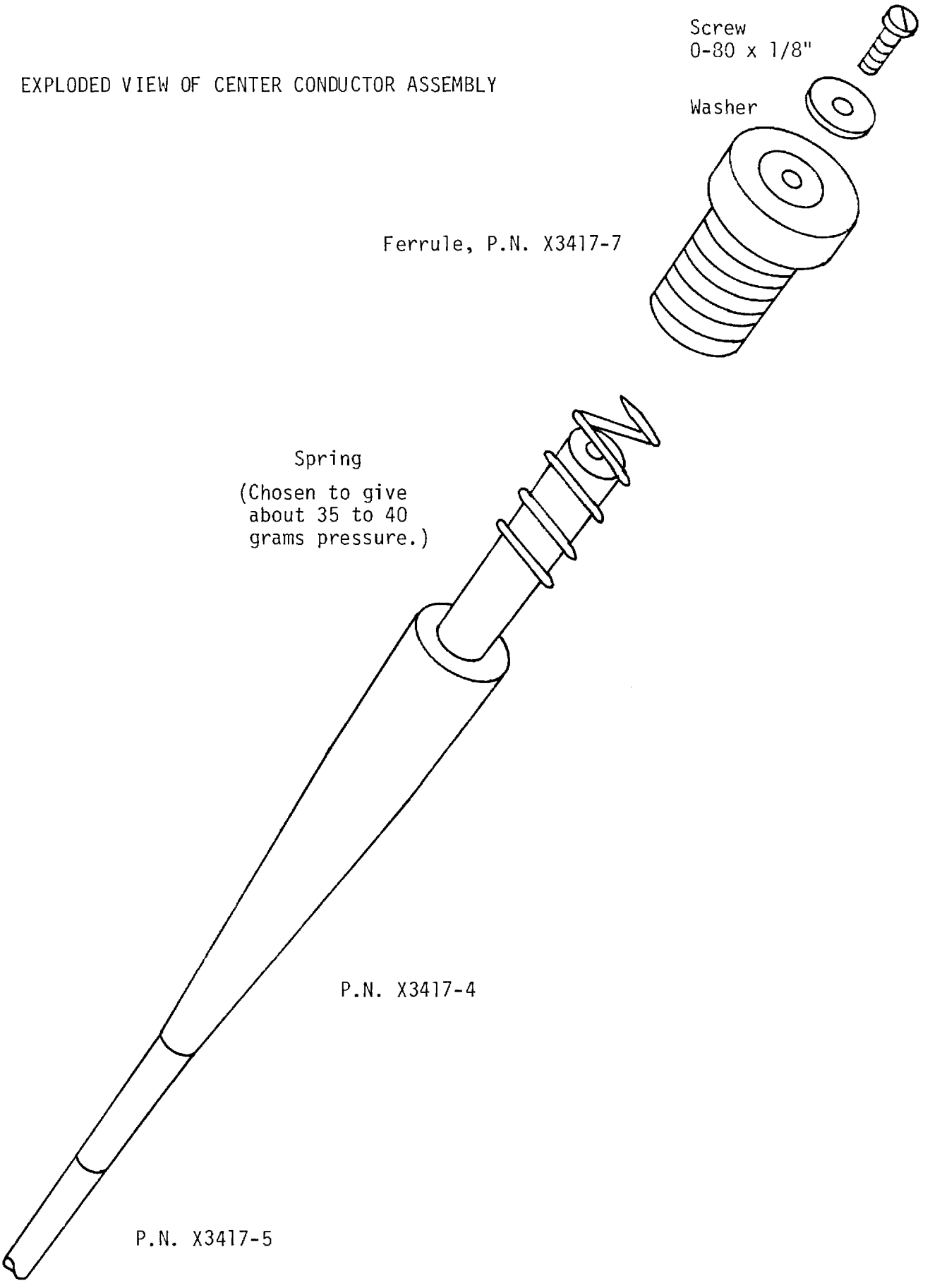
Notes:

1) Smooth slide fit in P.N. X3417-1

2) Rough machine teflon sleeve ≈.110 I.D., .159 O.D, x.240 LONG
Press into aluminum and swedge ends.
Machine I.D. to ≈.120 (Tight slide fit on P.N. 3417-5)

MAT'LS: Aluminum
Teflon

EXPLODED VIEW OF CENTER CONDUCTOR ASSEMBLY



MATERIALS X-BAND
X3417-(1-8)

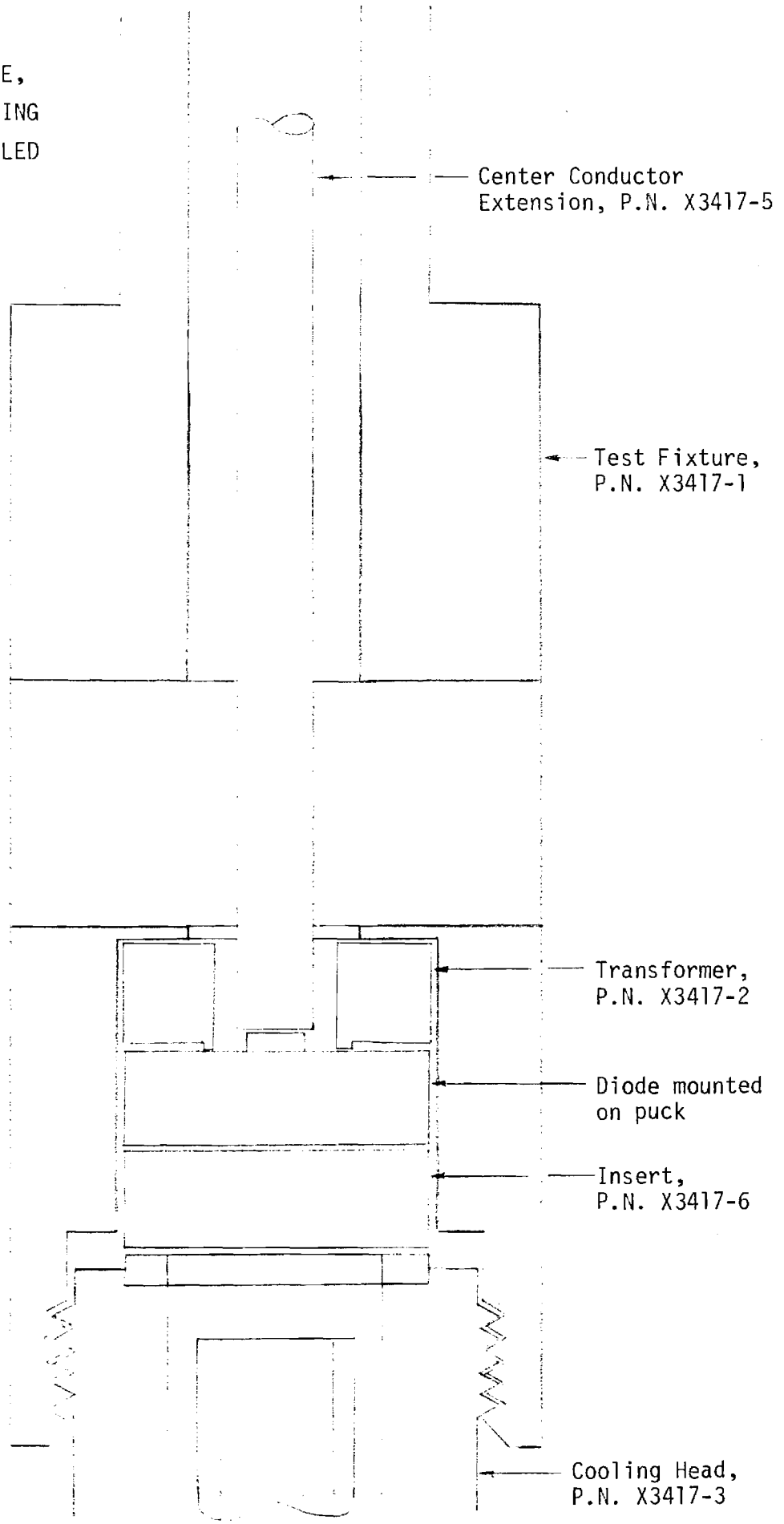
X-BAND

TEST FIXTURE

MATERIALS:

P/N	Material	Size
X3417-1	Aluminum	7/8 x 4 x 1-3/4
-2	Copper	1" long x 1/2 dia.
-3	Yellow Brass	1-3/4 long x 7/8 dia.
-4	Copper	3 long x 1/8 dia.
	Absorber	2-1/2 long x 3/8 dia.
-5	Copper	2 long x 1/8 dia.
-6	Copper	1 long x 1/2 dia.
-7	Nylon	1-1/2 long x 3/4 dia.
-8	Aluminum	1 long x 3/8 dia.
	Teflon	1 long x 3/16 dia.

SIDE VIEW OF TEST FIXTURE WITH DIODE, MATCHING AND COOLING ASSEMBLIES INSTALLED



A-2351

Monthly Status Letter No. 4

Evaluation and Assembly of X-Band Pulsed GaAs IMPATT Diode Chips

P.O. No. P0163130

Contract period covered
11 June 1979 through 10 July 1979

Submitted to

General Dynamics
Pomona Division
Pomona, California 91766

by

Solid State Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting through

Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

Prepared by

C.T. Rucker
W.K. Parks

17 July 1979

INTRODUCTION

This status letter reports progress in the series connection of X-band IMPATT diodes (lot No. VSX9251AM). Work done from June 11 through July 10, 1979, is summarized. During the early report period, four two-chip assemblies were fabricated, two of which were delivered to General Dynamics in accordance with contract provisions. Progress during the latter part of the report period was slowed considerably for two reasons. Two key personnel took annual leave during the period. Also, both the packages and diamonds on order to be used in the next phase of the project were delayed in shipping.

UNPACKAGED TWO CHIP ASSEMBLIES

Four two-chip diodes were fabricated and r.f. tested this month. Diode assembly VSX9251AM-H (chips #5 and #9) failed under r.f. test after dropping mode at low current (1.0 amp). The following data were the last taken before mode drop:

[volts]	[Amp]	[watt]	[watt]	[%]	[GHz]	[μsec]	[%]
V	I	P	Po	η	fo	P.W.	Duty
~100	1.0	100	14.0	14.0	10.0	1	20

Diode VSX9251AM-I (chips #15 and #32) also failed after dropping mode at low current (0.9 amp). Again, the following data were taken before failure.

V	I	P	Po	η	fo	P.W.	Duty
99	0.8	76.0	14.0	18.4	9.8	1	20

The contact leads were then removed from VSX9251AM-H, and an SEM analysis was made. The accompanying photograph shows that the failure was due to an edge burnout of one of the diodes. It was assumed that the second assembly also failed due to this mechanism, and the entire assembly was

re-etched in a semiconductor etch to clean up the surface.

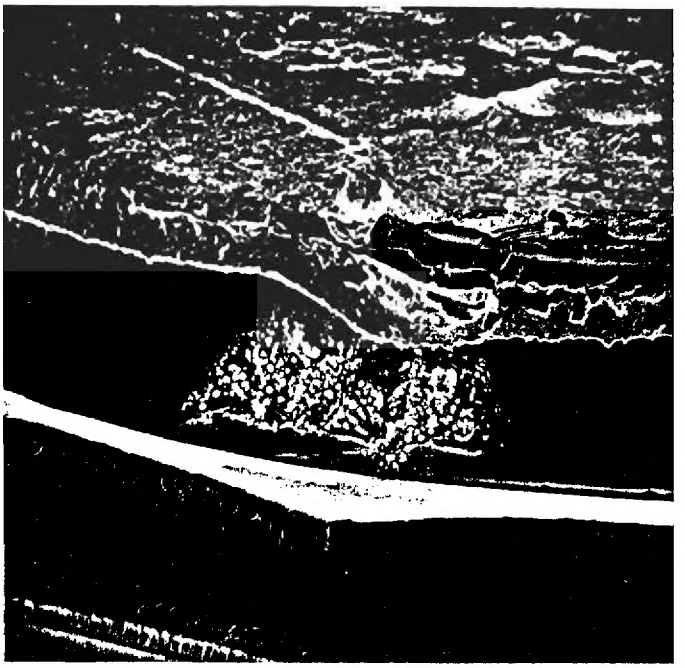


Figure 1. Two-Chip Assembly (VSX9251AM-H) Mag = 520x. Failed Diode Showing Edge Burnout.

The following data were then recorded on VSX9251AM-I:

V	I	P	Po	η	fo	P.W.	Duty
112	1.00	112	16.0	14.3	10.5	1	20

Additional r.f. testing on this diode indicated that the operating frequency could be pulled down to 10 GHz and below with a change of transformer in the test fixture.

The low operating current measured for the two diodes was disturbing in view of an average operating current of 1.47 amps for the six one and two-chip diodes which were r.f. tested (VSX9251AM-A,B,C,D,F). An examination of the d.c. characteristics of the individual diodes used in the

assemblies revealed nothing out of the ordinary. The values of breakdown voltage, the voltage difference between the high and low current breakdowns, and walkout of the diodes was similar to those observed for the diodes with higher operating currents.

In the previous assemblies, the bottom diode was electrically connected to the puck with a gold foil strap. The strap was left off diodes H and I, however, and replaced by a layer of gold metallization on one side of the diamond. It was thought that the low operating current might be due to high resistance in the metallization due, e.g., to a crack in the gold along the corner of the diamond. Such was not the case. When a ground strap was added to VSX9251AM-I after the r.f. testing indicated above, no increase in operating current was observed.

The tentative conclusion is that the low operating currents resulted from surface effects caused by the lack of a final cleanup etch subsequent to assembly, but prior to r.f. testing. The fact that VSX9251AM-I operated at 1.0 amp after an extended etch which reduced its size an estimated 30% suggests that, but for the surface effects due to lack of cleanup etch, it may have operated at much higher current.

Two more two-chip assemblies were then fabricated, VSX9251AM-J (chips #23 and #38) and VSX9251AM-K (chips #10 and #28).

VSX9251AM-J

V	I	P	Po	η	f_o	P.W.	Duty
96.0	1.30	125	17.3	13.8	10.3	1	20

VSX9251AM-K

V	I	P	Po	η	f_o	P.W.	Duty
107	1.30	139	24.1	17.3	9.9	1	20

The final cleanup etch was performed on these diodes, and no problems were encountered during testing. These diodes were forwarded to General Dynamics, along with a separate cover letter, on June 29, 1979.

With the delivery of these diodes, Phase I of the task was completed.

PLANS FOR NEXT MONTH

Phase II of the project involves the development of a packaged two-chip assembly and a study of various operating characteristics including parasitics, thermal interaction and operating frequency adjustment. Although the proposal calls only for two-chip assembly, a three-chip assembly is also planned for this phase in order to partially compensate for the low output power produced by diodes from this lot.

The 80 mil diameter packages to be used in Phase II have arrived, but the diamonds to be used in the three-chip fabrication have been delayed. The diamonds are not regularly stocked by the vendor, and must be specially cut. They are on order, but will not be received for another 9 to 11 weeks from the date of this letter. When they arrive, a three-chip assembly will be built. However, for the next period, a two-chip assembly will be built, tested, and evaluated in the 80 mil packages with standard diamonds on hand.

A 2357

Monthly Status Letter No. 5

Evaluation and Assembly of X-Band Pulsed GaAs IMPATT Diode Chips

P. O. No. PO163130

Contract period covered
11 July 1979 through 10 August 1979

Submitted to

General Dynamics
Pomona Division
Pomona, California 91766

by

Solid State Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting through
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

Prepared by

C. T. Rucker
W. K. Parks

21 August 1979

INTRODUCTION

Work done from July 11 through August 10, 1979 on the series connection of X-band IMPATT diodes (Lot No. VSX9251AM) is reported in this status letter. The first section gives results of tests of the first two packaged two-chip assemblies which were fabricated - neither of which performed satisfactorily. The second section and its corresponding Appendix tabulate the disposition of the diodes used to date in the program, and summarizes the performance of the assemblies which have already been built and RF tested. An analysis of several dc characteristics of the individual chips is also included in the section in an attempt to isolate those which best predict the RF performance of the diode. The third section presents the overall administrative status (including scheduling and funding) of the program. Plans for next month are then outlined.

PACKAGED ASSEMBLIES

As mentioned in Monthly Status Letter No. 4, both two- and three-chip assemblies are being developed in Phase II of the program. The three-chip assemblies require mounting diamonds of size 1 x 1.5 x 0.5 mm and packages with a 2 mm (80 mil) diameter center hole—type AV174-1. The packages were received last month, but the diamonds, although they have been on order for some time, are not scheduled for delivery until five to seven weeks from the date of this letter. The tentative plan was to build a three-chip assembly first. Because smaller 1 x 1 x 0.5 mm diamonds were already on hand, two two-chip assemblies were fabricated using these diamonds in the AV174-1 package. Both assemblies, however, failed during the initial stages of RF testing.

Because of the large physical size of the package, the RF test fixture was not used in the Kurokawa configuration (i.e., using a puck with a hole drilled in the center as a matching transformer), but a top hat was used instead to provide matching. For proper operation, the transformer should extend beyond the top lid of the package when mounted in the fixture. Also the center hole of the transformer must be large enough to accommodate the package. From past experience, it was feared that a transformer with such large dimensions would pull the frequency of operation far below X-band.

Assembly VSX9251AM-L (chips #4 and #11) was fabricated in the package and the RF tested. The input current was increased slowly to 0.4 Amp, whereupon the top diode failed. The device never produced any output power, and no RF data were taken. Because the chips were obscured by the package, an SEM analysis was not feasible. However, it was determined that the diode did not fail due to edge burnout.

VSX9251AM-M (chips #12 and #24) was built and tested next. Low power oscillation was obtained with an input current of 0.25 Amps. At that current and during the initial matching effort, the diode failed after dropping mode. Again no RF data were taken.

Because the other chips in this lot operated at input currents on the order of 1.5 Amps, failure at such low current levels is disturbing. There is the possibility that there is a microwave circuit problem which exists due to the new device geometry and its interaction with the top hat matching in the test fixture. Tests with different size hats are planned, and if it appears necessary, a transformer will be used for matching instead of the hat.

However, as pointed out in the succeeding section, chips with a moderate amount of premature breakdown tend to fail more readily during

RF test than those with less. Because of the statistically small number of chips which have been tested, this premise is only tentative. Also it cannot provide the complete explanation for these two failures, because none of the other diodes with premature breakdown failed at such extremely low current. In any event, an assembly should be built with chips showing sharp breakdown to eliminate possible failure due to premature breakdown.

DIODE CHIP STATUS

Of the fifty chips supplied at the start of this program, twenty-two chips remain both operational and unused in diode fabrication. Of the other twenty-eight chips, three failed during preselection, twenty-four were used in assemblies and one was destroyed during fabrication of the assemblies.

A total of thirteen assemblies have been built, and they breakdown as follows:

Type	Package	# Built	# Still Operating
One-Chip	N-57	2	1
One-Chip	N-33	1	1
Two-Chip	None	7	3
Two-Chip	AV174-1	2	0
Three Chip	None	1	1*

*Converted to two-chip assembly after one chip failed.

Appendix I presents a more detailed summary of the disposition of the diodes and summarizes both the dc characteristics of the single chips and the RF operating characteristics of the completed assemblies. Four dc characteristics are included in the Appendix - premature breakdown, walkout, ballooning, and slope parameter.

Premature breakdown usually results from a defect or localized non-uniformity in the semiconductor which causes that portion of the reverse biased diode to break into conduction at a lower voltage than the rest of the diode. Walkout is a measure of the difference in breakdown voltage at low and high currents. Ballooning describes the thermal hysteresis observed at high current. As the voltage is increased until the diode conducts a given current, the junction is heated. As the voltage is then decreased, the junction still remains heated, and the breakdown voltage associated with a given current is smaller in magnitude. Proper heat sinking on the diode will decrease the size of this thermally induced hysteresis or "balloon" in the diode's I-V curve.

The I-V curves for the fifty chips were examined, and the amount of each of these three unwanted characteristics for each chip was labeled as slight (S), moderate (M), or excessive (E). Figures 1 and 2 illustrate the classification scheme for chips #1, 2, 19, and 20.

The fourth characteristic, slope parameter, is a merit figure of sorts, and is defined in Figure 3. As the value of the parameter increases, the diode's merit decreases.

The data of Appendix I were investigated for a connection between dc characteristics and RF performance. The two-chip assembly which failed due to coolant leak (VSX9251AM-G) was excluded from the analysis. Of the twenty-two chips actually used in the devices assembled, excluding VSX9251AM-G, eight chips failed during RF test. The histograms of Figures 4-6 plot the failed diodes and the diodes actually used against dc characteristics. Although the data are much too sketchy to be conclusive, certain tendencies should be noted.

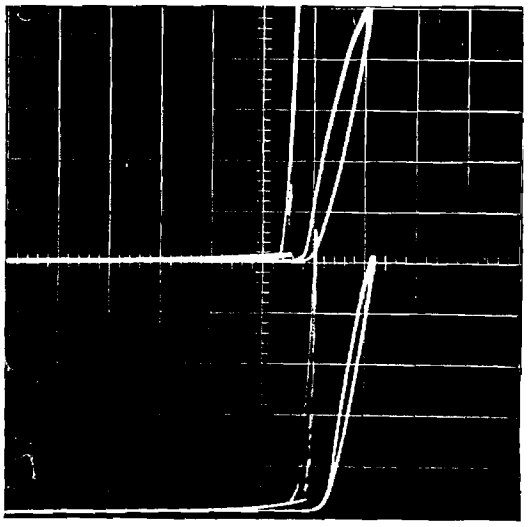


Figure 1. DC Characteristics.

Vertical 1 = 0.2 mA/division
Vertical 2 = 10 mA/division
Horizontal = 5 V/division

	P.B.	W.O.	Balloon
Top (chip #2)	S	S	M
Bottom (chip #1)	M	S	S

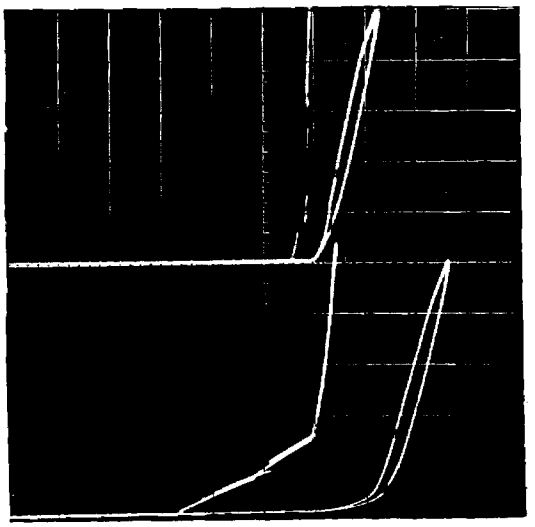


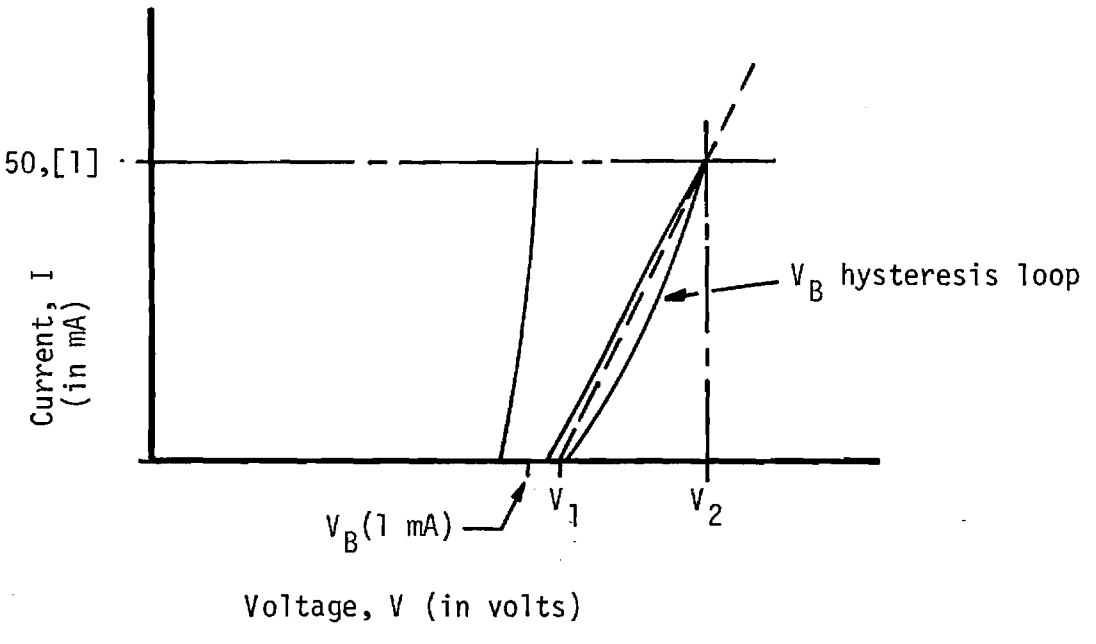
Figure 2. DC Characteristics.

Vertical 1 = 0.2 mA/division
Vertical 2 = 10 mA/division
Horizontal = 5 V/division

	P.B.	W.O.	Balloon
Top (chip #20)	S	S	S
Bottom (chip #19)*	E	E	S

P.B. = Premature Breakdown
W.O. = Walkout
E = Excessive
M = Moderate
S = Slight

*Chip #19 data shown here was taken before etching and does not agree with data after etching the diode as recorded in Appendix I.



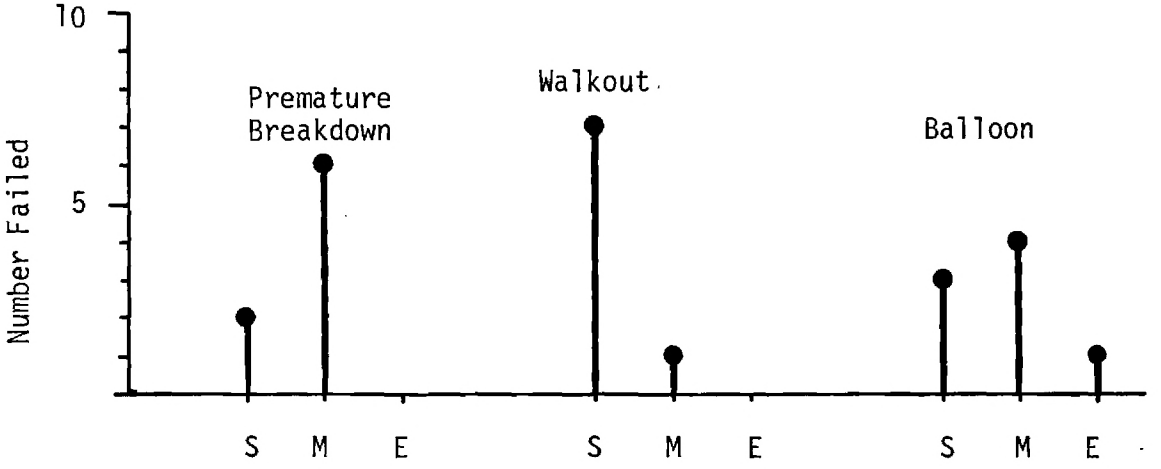
V_B(1 mA) - the breakdown voltage measured at I = 1 mA.

$V_1 = V_B$(intercept) - defined in sketch above.

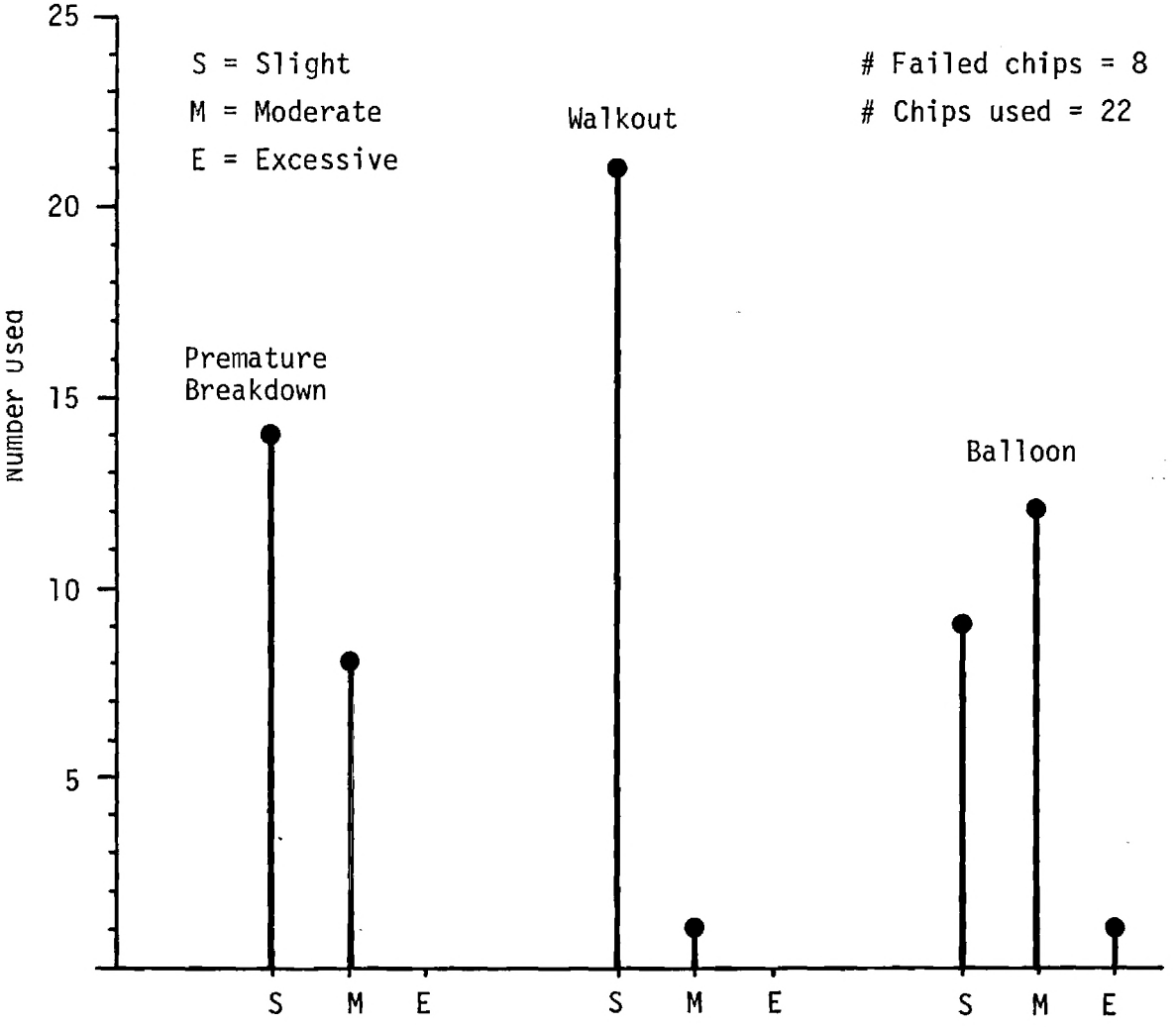
$V_2 = V_B$(50 mA) = the breakdown voltage measured at I = 50 mA.

$$\text{Slope Parameter, } F = \frac{2(V_2-V_1)}{(V_1+V_2)}$$

Figure 3. Definition of Slope Parameter

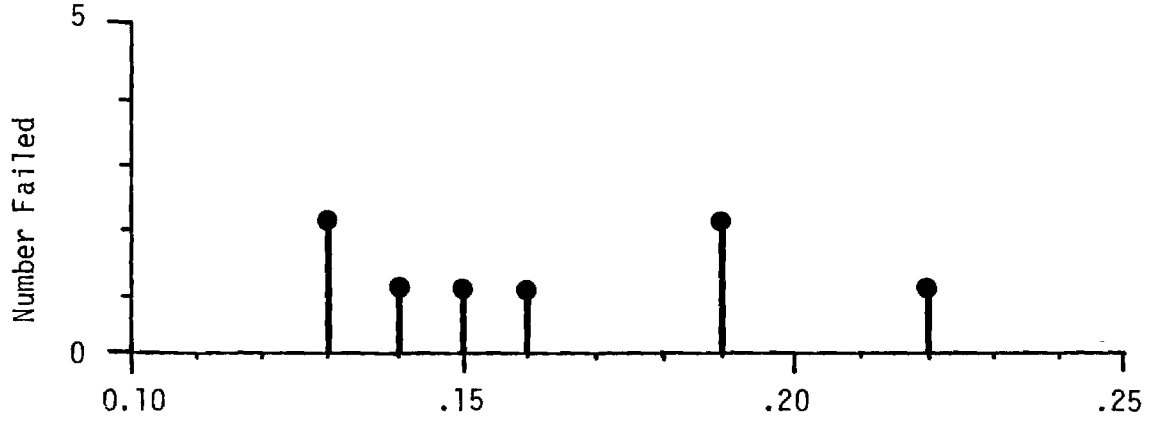


(a) Occurrence vs. dc Characteristics for Failed Chips

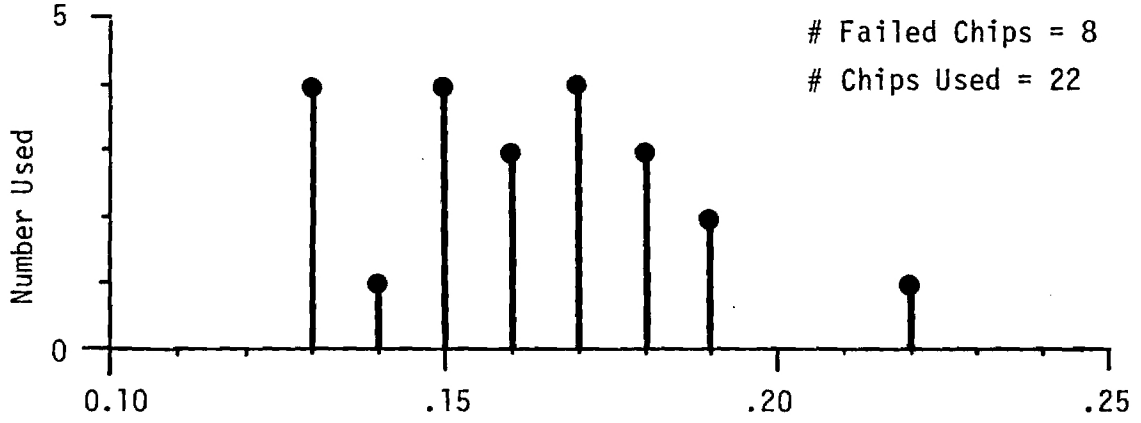


(b) Occurrence vs. dc Characteristics for all Chips Used

Figure 4. DC Characteristic Histogram

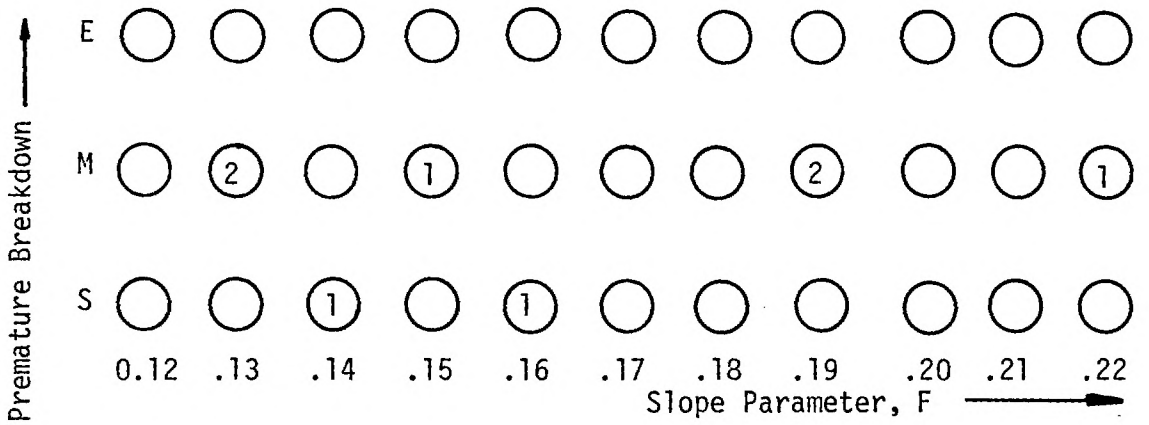


(a) Occurrence v s. Slope Parameter, F, for Failed Chips

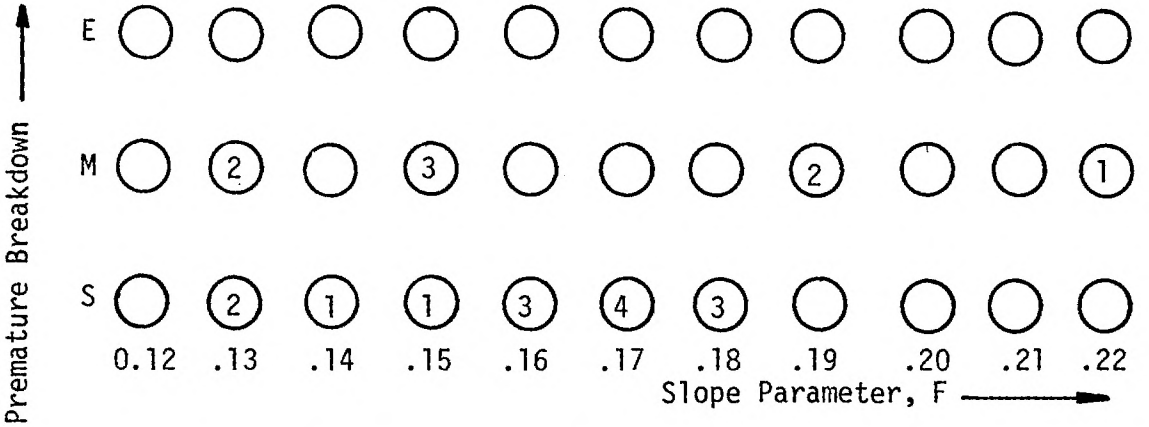


(b) Occurrence vs. Slope Parameter, F, for all Chips Used

Figure 5. Slope Parameter Histogram



(a) Occurrence vs. Premature Breakdown and Slope Parameter, F, for Failed Chips



(b) Occurrence vs. Premature Breakdown and Slope Parameter, F, for all Chips Used.

Figure 6. Joint Premature Breakdown/Slope Parameter Histogram. The numbers in the circles give the number of occurrences for a given combination of premature breakdown value and slope parameter, F.

Diode failure does not appear to be related to the ballooning parameter of the individual chip. This agrees with what has been noticed during fabrication: attaching chips with large loops to pucks or packages drastically decreases the amount of hysteresis. The fact that both the failures and diodes used are distributed evenly across the ballooning parameter reinforces the observation made in practice.

Because twenty-one of the twenty-two chips surveyed exhibited the same amount of walkout (slight), it is obvious that this parameter is not the cause of the failures. Premature breakdown, however, is a different story. Of the fourteen diodes used with slight premature breakdown, only two failed (14.3%); of eight used with moderate breakdown, six failed (75%).

In Figure 5, no pattern is evident in the display of failed diodes versus slope parameter, F. Both the overall chips used and failed chips are distributed evenly over the parameter. Figure 6 shows the failed chips plotted simultaneously against slope parameter and premature breakdown. Again the only pattern evident is the tendency for diodes with higher premature breakdown to fail more readily than those with slight.

Because of the possible correlation between premature breakdown and RF failure, two of the chips with excessive breakdown (#19 and #21) were etched to try to improve the sharpness of breakdown. The V-I curve of #19 before etching was already shown in Figure 2. The pre-etch characteristics of #21 are shown in Figure 7. The characteristics of the diodes after etching are presented in Figure 8.

The premature breakdown of chip #19 was improved by the etching, but no change was seen in #21. A possible explanation for this result is that the defect or localized nonuniformity is located randomly within

Oscilloscope Settings
for Figures 7 and 8.

Vertical 1 = 0.2 mA/division
Vertical 2 = 10 mA/division
Horizontal = 5 V/division

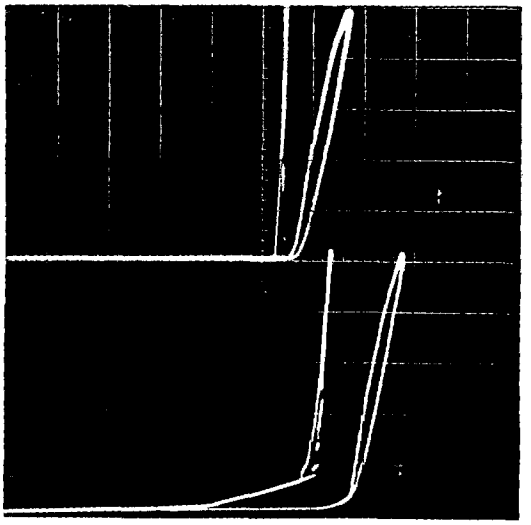


Figure 7. Pre-etch dc Characteristics.

	P.B.	W.O.	Balloon
Top (chip #22)	S	S	M
Bottom (chip #21)	E	S	E

the subject diode. If the defect(s) in #19 was close to the surface, it would be removed during the etch; if the defect(s) in #21 was further from the surface, it would not be affected by the etch. Other diodes in this lot have actually had the sharpness of breakdown degrade slightly when etched. Again, such a situation might occur if the defect(s) was away from the surface. Then the portion of the diode without defects would be decreased during etching, while the volume with defects remained constant. The relative effect of the defect would be larger, and the premature breakdown would be enhanced. In sum, there is no guarantee that any of the chips with premature breakdown can be improved by etching.

Working on the premises that diodes with premature breakdown fail more readily under RF test and that they cannot be improved with etching, the majority of the remaining chips are unsuitable for use in packaged two-chip assemblies. Of the twenty-two remaining, only six have slight premature breakdown (#8, 19, 30, 40, 43, 44). Of these, five have excessive values of walkout or ballooning (#8, 19, 30, 40, 43). Thus, there is no ideal pair remaining for building a two-chip assembly. For the next period, another packaged two-chip assembly is planned using two chips (#14 and #17) with moderate premature breakdown.

However, as already mentioned, a package assembly using chips with sharp breakdown needs to be constructed. Toward this end, an additional group of fifty diodes from the same Varian lot has been requested by C. Rucker in telephone conversation with C. Mason of General Dynamics. Upon their receipt, preparation for building the two-chip assembly will begin immediately.

GENERAL CONTRACT STATUS-SCHEDULE AND FUNDING

Contract Phases, content, funding and schedule are summarized below for reference purposes. Contract start date was February 1979.

Phase	Content	Funding	Scheduled Completion Date
I	Diode Evaluation	$ 9,534	5/31/79
II	Package Evaluation/ Development	$10,474	7/31/79
III	Fabricate Multipchips	$11,990	9/28/79

At present, Phase I diode evaluation is complete (50 chips supplied by General Dynamics). Phase II has been started using chips from this device lot but further progress requires additional chips. Fifty additional chips were requested from C. Mason on 16 August 1979.

Clearly, Phase II is not complete on schedule. The primary reason for slippage involves the extraordinary effort spent in attempting to achieve RF performance as specified by the chip vendor. The specified performance has not been achieved even with the heavy effort. The multi-chip tasks have been continued nevertheless at the available performance levels by mutual agreement between General Dynamics and Georgia Tech personnel.

To continue with Phase II, the second chip lot must be evaluated (see footnote, page 3, Georgia Tech Proposal AS-SSS-1907). Then, additional experiments related to the packaged multichips can be performed. The estimated new Phase II completion date, assuming receipt of additional chips by 24 August 1979, is 26 October 1979, leading to an estimated Phase III completion date of 18 January 1980.

Funds remaining on 31 July 1979 are $17,094.52. Some of the detailed tasks, noted under Phase II, Proposal AS-SSS-1907, have already been accomplished with funding available on other efforts. Therefore, it appears possible that Phases II and III can be completed with the funds presently authorized. Therefore, additional funds are not requested at this time.

Schedule extensions are presently being requested via Georgia Tech Contracts and C. B. Gleason.

PLANS FOR NEXT MONTH

- Preselection and evaluation of new batch of fifty chips expected to be received this month.
- Continued fabrication of two-chip packaged assemblies using chips from both the first and second batch of diodes. Work on the three-chip assembly would also be planned, except delivery of the 1 x 1.5 x 0.5 mm mounting diamonds is not expected until five to seven weeks from the date of this letter.
- If appropriate, some of the remaining single chips in the first batch will be put into packages and RF tested to add to the data correlating dc characteristics with RF performance.

APPENDIX I.

Chip Usage Summary

DIODE LOT VSX 9251AM

GENERAL DYNAMICS

Summary 8/16/79

Chip No.	dc Characteristics				Use			Op. Status		Comments
	P.B.	W.O.	Balloon	F	Con.	Dsg.	Pkg.	Chip	Assy	
1	M	S	S	0.135	N57	B	Yes	No	No	Assy. dropped mode.
2	S	S	M	.171	N33	A	No	Yes	Yes	RF performance satisfactory
3	S	S	S	.131	N57	C	No	Yes	Yes	Low RF efficiency
4	M	M	M	.190	1x2	L	Yes	No	No	Assy. failed at 0.4 Amp
5	M	S	S	.154	1x2	H	No	No	No	Assy. failed at 1.0 Amp
6	S	M	M	.140	1x3	D	No	No	No	Assy. converted to 1x2
7	M	M	M	.212						Unused
8	S	S	M	.198						Unused
9	M	S	S	.130	1x2	H	No	No	No	Assy. failed at 1.0 Amp
10	S	S	M	.178	1x2	K	No	Yes	Yes	Delivered to General Dynamics
11	S	S	M	.186	1x2	L	Yes	Yes	No	Assy. failed at 0.4 Amp, No RF
12	M	S	M	.190	1x2	M	Yes	No	No	Assy. failed at 0.25 Amp
13	M	M	E	.245						Unused
14	M	S	M	.211						Unused
15	S	S	M	.171	1x2	I	No	Yes	Yes	Assy. operational after re-etch
16	S	S	S	.150	1x3	D	No	Yes	No	Assy. converted to 1x2
17	M	S	S	.162						Unused
18	M	E	E	.259						Unused
19	S	E	E	.323						Unused
20	S	S	S	.165	1x2	E	No	Yes	No	Assy. failed at 0.6 Amp
21	E	M	E	.211						Unused

Chip No.	dc Characteristics				Use			Op. Status		Comments
	P.B.	W.O.	Balloon	F	Con.	Dsg	Pkg.	Chip	Assy	
22	S	S	M	.161	1x2	E	No	No	No	Assy. failed at 0.6 Amp.
23	S	S	S	.131	1x2	J	No	Yes	Yes	Delivered to General Dynamics
24	S	S	M	.180	1x2	M	Yes	Yes	No	Assy. failed at 0.25 Amp.
25	M	E	M	.237						Unused
26										Chip failed during preselection
27	M	M	M	.170						Unused
28	S	S	M	.186	1x2	K	No	Yes	Yes	Delivered to General Dynamics
29	M	S	E	.226	1x2	F	No	No	No	Assy. failed at 1.5 Amp.
30	S	S	M	.190						Unused
31										Chip failed during preselection
32	S	S	M	.161	1x2	I	No	Yes	Yes	Assy. operational after re-etch
33	M	S	E	.209						Unused
34	M	M	M	.175						Unused
35	M	S	S	.154	1x2	F	No	Yes	No	Assy. failed at 1.5 Amp
36	S	S	M	.226						Chip destroyed during fabrication
37	M	S	S	.128	1x2	G	No	Yes	No	Assy. failed to coolant leak
38	M	S	S	.156	1x2	J	No	Yes	Yes	Delivered to General Dynamics
39	E	M	M	.170						Unused
40	S	M	E	.131						Unused
41	M	E	M	.185						Unused
42	M	E	M	.188						Unused
43	S	S	M	.171						Unused
44	S	S	E	.292						Unused
45	M	S	M	.151						Unused
46										Chip failed during preselection

Chip No.	dc Characteristics			Use				Op. Status		Comments
	P.B.	W.O.	Balloon	F	Con.	Dsg.	Pkg.	Chip	Assy.	
47	S	S	M	.177	1x3	D	No	Yes	No	Assy. converted to 1x2
48	S	S	M	.187	1x2	G	No	No	No	Assy. failed due to coolant leak
49	S	S	S	.173						Unused
50	M	S	M	.194						Unused

Legend: P.B. = Premature Breakdown
W.O. = Walkout
F = Slope Parameter
Con. = Configuration
Dsg. = Designation, e.g. "A" means the chip was used in assembly VSX9251AM-A
Assy. = Assembly
Op. Status = Operational Status, i.e., is the chip (or assembly) still working?
E = Excessive
M = Moderate
S = Slight

Monthly Status Letter No. 6

Evaluation and Assembly of X-Band Pulsed GaAs IMPATT Diode Chips

P.O. No. P0163130

Contract period covered
11 August 1979 through 10 September 1979

Submitted to

General Dynamics
Pomona Division
Pomona, California 91766

by

Solid State Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting through

Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

Prepared by

C.T. Rucker
W.K. Parks

14 September 1979

INTRODUCTION

Work done from August 11, through September 10, 1979, on the series connection of X-band IMPATT diodes (Lot No. VSX9251AM) is reported in this Status Letter. During the report period, a two-chip and a three-chip packaged assembly were fabricated and RF tested. For these devices, diodes from the initial group of fifty supplied at the beginning of the program were used. Because of the relatively poor dc characteristics of the remaining chips, device fabrication was suspended until the arrival of the second group of fifty diodes on the last day of the report period.

PACKAGED ASSEMBLIES

Following the failure of the first two two-chip packaged assemblies (VSX9251AM-L and -M), a third one was built (VSX9251AM-N). A 1 x 1 x 0.5 mm diamond and AV174-1 package were used for the assembly. For the RF test, the top hat fixture was initially used with a fairly large top hat (length = 0.151", diameter = 0.231"). The following data were taken before the cover was placed on the packaged assembly.

[volt]	[Amp]	[Watt]	[Watt]	[%]	[GHz]	[μsec]	[%]
V	I	P	P_o	η	f_o	P.W.	Duty
112.0	0.95	106.4	19.6	18.5	9.10	1	20

Using the same test fixture, the efficiency and power output dropped slightly when the cover was attached.

In order to increase the operating frequency, a smaller top hat (length = 0.150", diameter = 0.120") was tried. With extensive tuning, the following data were obtained:

V	I	P	P_o	η	f_o	P.W.	Duty
104.0	0.75	78.0	15.4	19.7	9.73	1	20

Although the power output available is low, the figures for efficiency and operating frequency are encouraging.

The next step was to build a three-chip assembly in the AV174-1 package. The special order diamonds, 1 x 1.5 x 0.5 mm, arrived well ahead of schedule, and the first three-chip (VSX9251AM-0) was assembled. Figure 1 is an SEM photograph of the device with the cover lid removed. During the initial

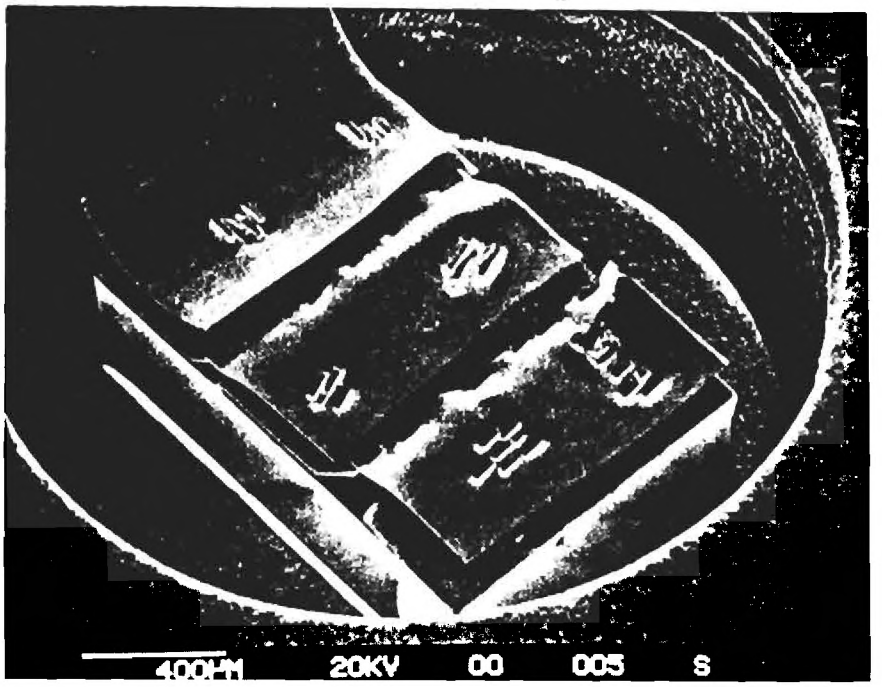


Figure 1. Three-Chip Assembly VSX9251AM-0. Nominal Geometry of Three-Chip Device.

RF test, the assembly failed at low current (I ~ 0.35 A) when the bottom diode developed an edge burnout. An SEM photograph of the failed diode is shown in Figure 2.

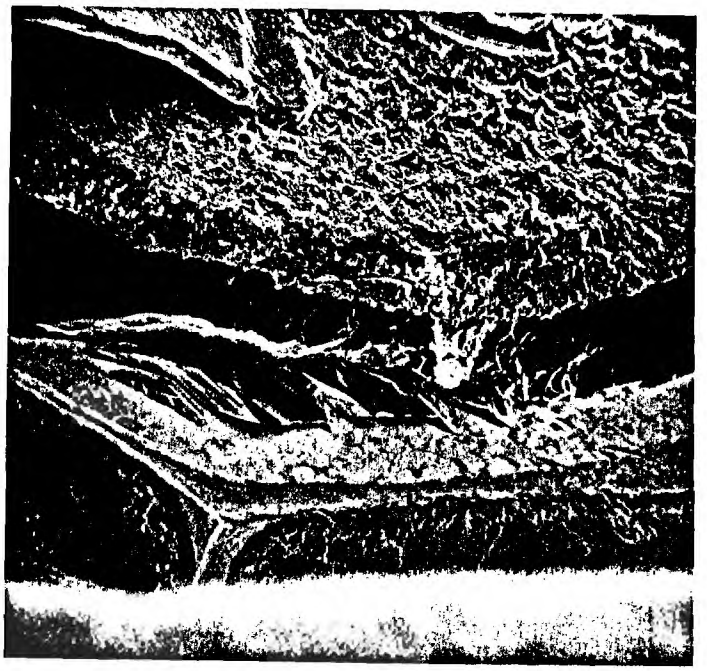


Figure 2. Three-Chip Assembly VSX9251AM-0. Mag. = 380x. Closeup of Failed Bottom Diode, Chip #43.

Semiconductor etching solutions were used to remove the burnout, but they also decreased the area of each chip by an estimated 50%. This reduction in device area lowered the current and output power expected from the assembly as well as the optimum pulse width and duty cycle for proper operation.

A second RF test was conducted on the assembly, and a number of combinations of pulse width and duty cycle were tried before the device failed

a second time. The second failure was a major one, with all three chips shorting. The best data recorded for the device were as follows:

V	I	P	P_o	η	f_o	P.W.	Duty
170.	0.50	85.0	9.8	11.5	9.74	0.4	8.0

Although the current and power output figures may look poor at first glance, it must be reiterated that the chips were etched to a fraction of their original area. The efficiency of the diode is not, however, a direct function of area. The low value of efficiency may be due to the fixed capacitance in parallel with each chip. When the chips were etched so that their area and corresponding capacitance were reduced, the parallel capacitors remained unchanged and no longer represented a proper choice for the device under test.

PLANS FOR NEXT MONTH

On September 10, the second group of fifty diodes from Lot VSX9251AM was received. Work next month will center on these chips including

- Preselection and evaluation.
- Fabrication and test of two- and three-chip packaged assemblies.

H-2351

Monthly Status Letter No. 7

Evaluation and Assembly of X-Band Pulsed GaAs IMPATT Diode Chips

P.O. No. P0163130

Contract period covered
11 September 1979 through 10 October 1979

Submitted to

General Dynamics
Pomona Division
Pomona, California 91766

by

Solid State Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting through

Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

Prepared by

C.T. Rucker
W.K. Parks

26 October 1979

INTRODUCTION

Work done from September 11 through October 10, 1979 on the series connection of X-band IMPATT diodes (Lot No. VSX9251AM) is reported in this Status Letter. During the report period, the new batch of fifty diodes was received and put through the preselection procedure. Three of these diodes were then used to fabricate a three-chip packaged assembly (VSX9251AM-P). The RF test of the assembly was not as rewarding as had been hoped -- maximum power and efficiency measured for the assembly was of the order of 22 watts at 13% efficiency.

PRESELECTION

The second batch of fifty chips was received at the beginning of the present report period. As in the first batch, the second batch was received in five containers of ten diodes each. Two adhesive identifying labels were placed inside each container, allowing the chips to be scrambled in the containers, with some of them adhering to the labels. The third container was one chip short of ten, and this diode was presumed lost in transit, probably due to the improper closure of the container caused by the labels.

Preselection on this batch of diodes was less extensive than that performed on the first batch. Preliminary SEM evaluation of "typical" chips was not done, because the general physical characteristics of the chips were determined in the analysis of the original batch of fifty. Initial capacitance measurements were also eliminated because the measurement is a routine part of the multichip fabrication process. Elimination of the measurement initially circumvents unnecessary handling of the diodes.

Table I presents the data obtained during preselection. Table II defines the parameters involved, and Figure 1 summarizes the data of Table I in

graphical fashion. Included for comparison as Figure 2 is the graphical summary of the data for chips 1-50 as it appeared in Status Letter #1. The diodes appeared to withstand the high current stress portion of the pre-selection process well -- only one diode failed.

RF TEST OF PACKAGED ASSEMBLY

From the diodes remaining after preselection, three were chosen with low breakdown voltages, matched values of ΔV, and reasonable premature breakdown characteristics (#67, 82, 88). A 1.0 x 1.0 x 0.5 mm diamond and AV174-1 package were used for the assembly. The package cover was left off the assembly during all RF tests. The first data taken were as follows:

VSX9251AM-P

[volt]	[Amp]	[watt]	[watt]	[%]	[GHz]	[μsec]	[%]
V	I	P	P_o	η	f_o	P.W.	Duty
166	0.90	149	19.2	12.9	9.1	1	20.

Using the same test fixture and top hat, the duty was lowered to see if more current could be applied to the assembly. The following data were recorded for duties of 15% and 10%:

V	I	P	P_o	η	f_o	P.W.	Duty
165	1.00	165	21.7	13.2	9.4	1	15.
157	1.28	201	20.7	10.4	9.6	1	10.

The duty was then returned to 20%, and data taken with the pulse width lowered to 0.75 μsec. The bottom diode in the assembly (#67) failed when the current was being raised above 0.80 Amps.

V	I	P	P_o	η	f_o	P.W.	Duty
158	0.80	126	15.1	11.9	9.3	0.75	20

From the RF tests, it appears that the 1 μsec pulse width is satisfactory, but that the 20% duty cycle is not optimum for the assembly. Assembly VSX0251AM-D tested earlier (Monthly Status Letter #2) was an unpackaged three-chip assembly in which the diamond was mounted directly on the puck for superior heat dissipation capability. Although the individual chips comprising Assembly P had lower breakdown voltages [avg. V_B(1 mA) = 28.5 versus 34.5v] and breakdown sharpness characteristics about as good as those of Assembly D, Assembly P would only support a current level of 0.9 Amps at 25% duty cycle while Assembly D ran at 1.5 Amps at 20% duty. Furthermore, Assembly P ran at successively higher current levels as the duty cycle was decreased -- as high as 1.28 Amps at 10% duty. These circumstances indicate that there may be a dissipation problem when the A174-1 package is simply screwed into the 1/2 inch puck.

Table III presents a survey of the maximum operating currents attained for the assemblies tested to date. Information for assemblies which never gave reasonable RF performance, but failed at extremely low output powers due to factors not related to current handling capabilities, has been left out of the table (e.g., failure due to coolant leak).

Due to the large number of variables affecting RF performance, nothing conclusive may be drawn from this Table; but it does appear that there may be over heating in the packaged multichip assemblies which limits the current capability when the packaged assembly is screwed into the puck.

One method of examining the possible heat dissipation problem is to make straightforward thermal resistance measurements of a single chip packaged diode screwed into the puck using heat sink grease and then to repeat the measurement with the same packaged diode soldered into the puck. A large difference between the two measurements would indicate a problem. Another method which may be the most effective is to perform the same tests on a three-chip assembly. If neither of these two tests locates the cause of the current limitation, then chip or microwave circuit factors will have to be examined.

PLANS FOR NEXT MONTH

- Fabrication of three-chip packaged assemblies.
- Investigation of operating current limitation caused by problems with either heat dissipation or, if appropriate, microwave circuit.

DIODE LOT: VSX9251

MANUFACTURER: VARIAN

LOT SUB NO.: E830

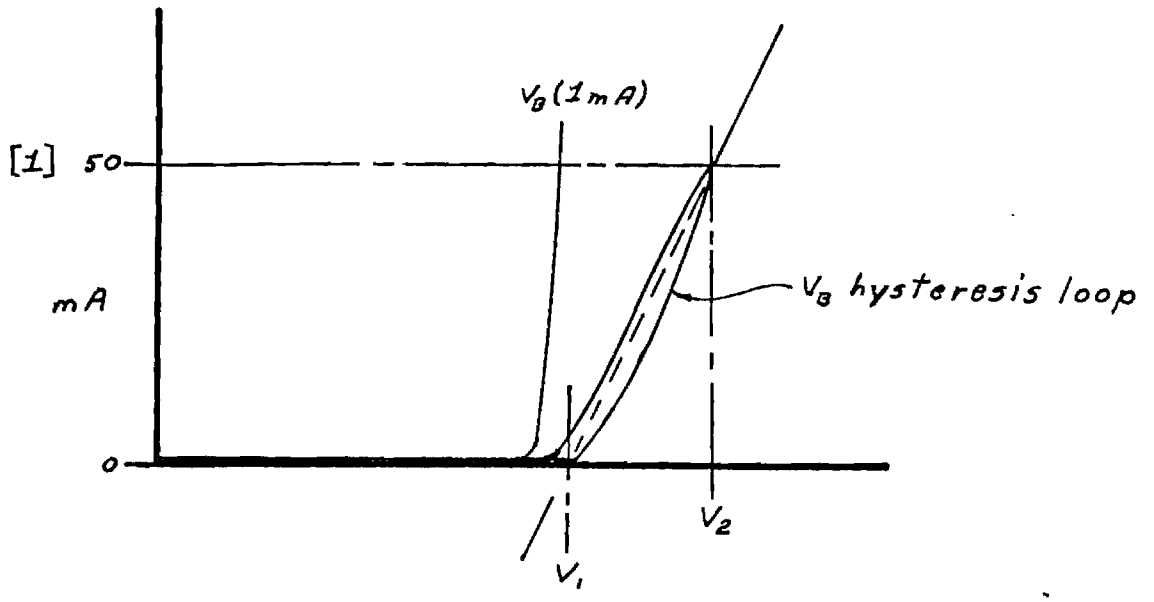
PRESELECTION SUMMARY

CHIP NO.	V_B(1mA)	V_1 V(Intercept)	V_2 V_B(50mA)	ΔV (V_2-V_1)	F $(\frac{2\Delta V}{V_1+V_2})$
51	29.5	31.5	36.5	5.0	0.147
52	38.0	39.0	47.0	8.0	0.186
53	34.5	36.5	46.0	9.5	0.230
54	42.0	44.0	53.0	9.0	0.186
55	34.5	41.0	50.0	9.0	0.198
56	▲				
57	31.0	32.5	37.0	4.5	0.129
58	38.5	37.5	48.5	11.0	0.256
59	*				
60	30.0	31.0	39.0	8.0	0.229
61	37.5	38.5	46.0	7.5	0.178
62	29.5	31.5	40.0	8.5	0.238
63	32.5	34.0	40.0	6.0	0.162
64	37.0	41.0	51.0	10.0	0.217
65	39.5	41.5	50.0	8.5	0.186
66	34.5	36.0	42.5	6.5	0.166
67	29.0	31.0	35.5	4.5	0.135
68	32.0	33.0	39.0	6.0	0.167
69	39.5	41.0	48.5	7.5	0.168
70	32.0	33.0	38.5	5.5	0.154
71	30.0	31.5	36.0	4.5	0.133
72	35.5	37.0	42.5	5.5	0.138
73	30.0	33.5	39.0	5.5	0.152
74	31.0	32.0	37.5	5.5	0.158
75	35.0	36.5	44.0	7.5	0.186
76	34.5	35.5	42.5	7.0	0.179
77	31.5	38.5	46.5	8.0	0.188
78	35.0	35.5	41.5	6.0	0.156
79	35.6	36.5	43.5	7.0	0.175
80	●				
81	35.5	36.0	42.0	6.0	0.154
82	28.5	29.5	34.0	4.5	0.142

DEFINITION OF PRESELECT PARAMETERS

V_B(1 mA) - the breakdown voltage measured at I = 1 mA. This current is usually sufficient to prevent erroneous V_B readings which sometimes result from premature breakdown and leakage.

V_1 = V_B(intercept) - defined as per sketch below.



PRESELECTION PARAMETERS

V_2 = V_B(50 mA) - the breakdown voltage measured at I = 50 mA. This stress level is usually sufficient to establish the rate of change and change in V_B due to current and associated heating.

F: $\frac{2(V_2-V_1)}{V_1+V_2}$ an arbitrary slope parameter defined as the change in V_B (ΔV) normalized to the average of V_2 and V_1. A merit factor of sorts.

Table II. Definition of Preselection Parameters

Assembly	Type	Package	I_{op}(max)	Duty
VSX9251AM-A	1-chip	N-33	1.25 Amps	20.%
B	1-chip	N-57	1.52	20.
C	1-chip	N-57	1.55	20.
D	3-chip	No	1.50	20.
"	3-chip	No	1.60	10.
"	2-chip	No	1.53	20.
F	2-chip	No	1.52	20.
H	2-chip	No	1.00	20.
I	2-chip	No	1.00	20.
J	2-chip	No	1.30	20.
K	2-chip	No	1.30	20.
L	2-chip	AV174-1	0.40	20.
M	2-chip	AV174-1	0.25	20.
N	2-chip	AV174-1	0.90	20.
O*	3-chip	AV174-1	0.25	20.
"*	3-chip	AV174-1	0.52	10.**
P	3-chip	AV174-1	0.90	20.
"	3-chip	AV174-1	1.00	15.
"	3-chip	AV174-1	1.28	10.

* This diode was etched to about 1/2 of its original area before it resumed operation after failure during the initial RF test.

** Pulse width - 0.3 μsec.

TABLE III

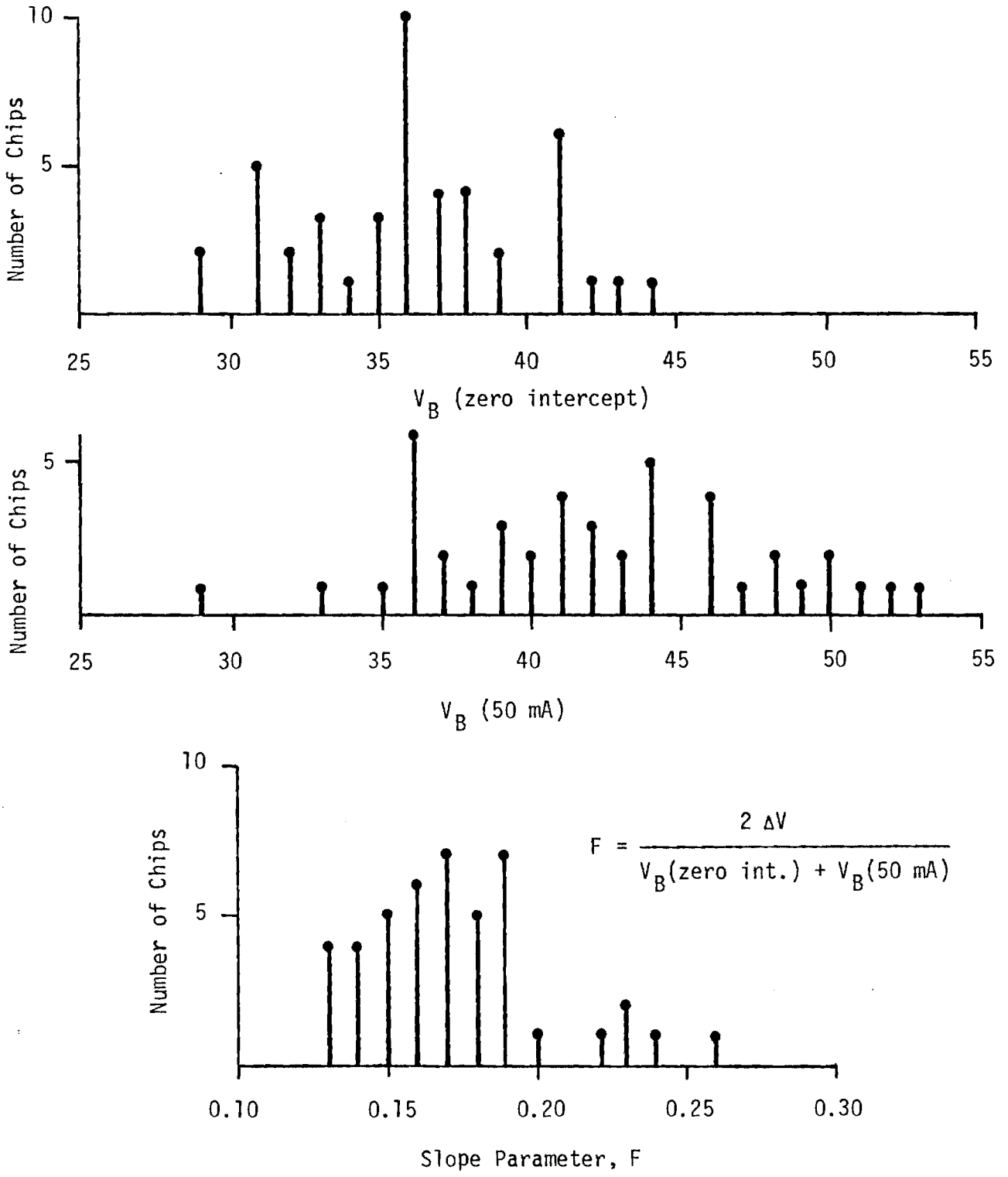
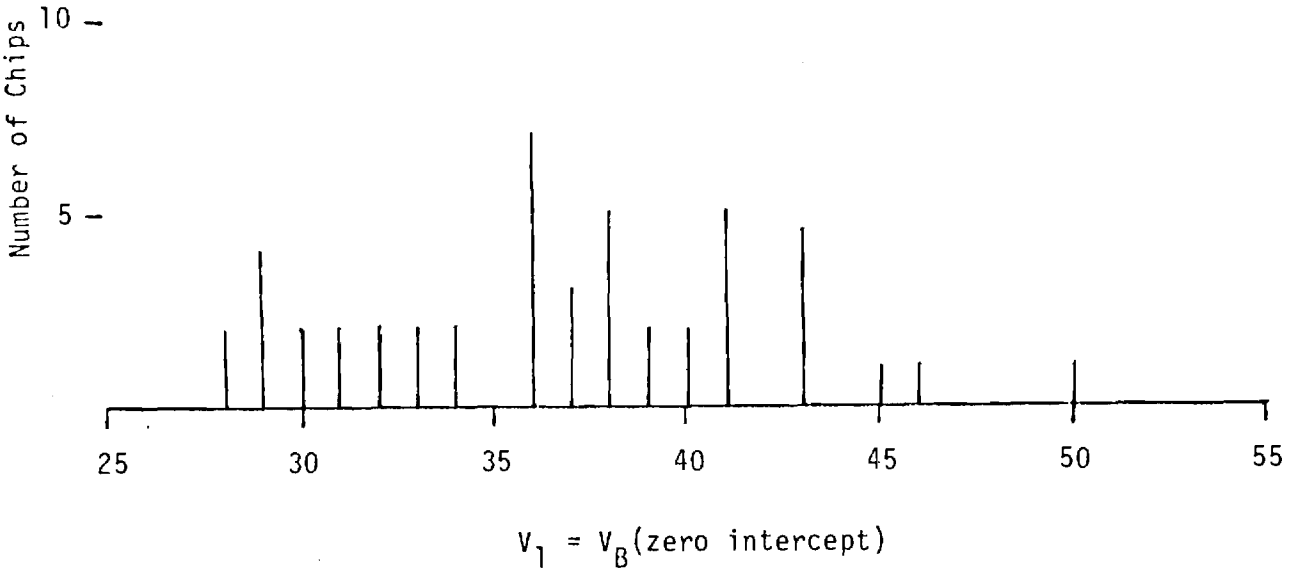
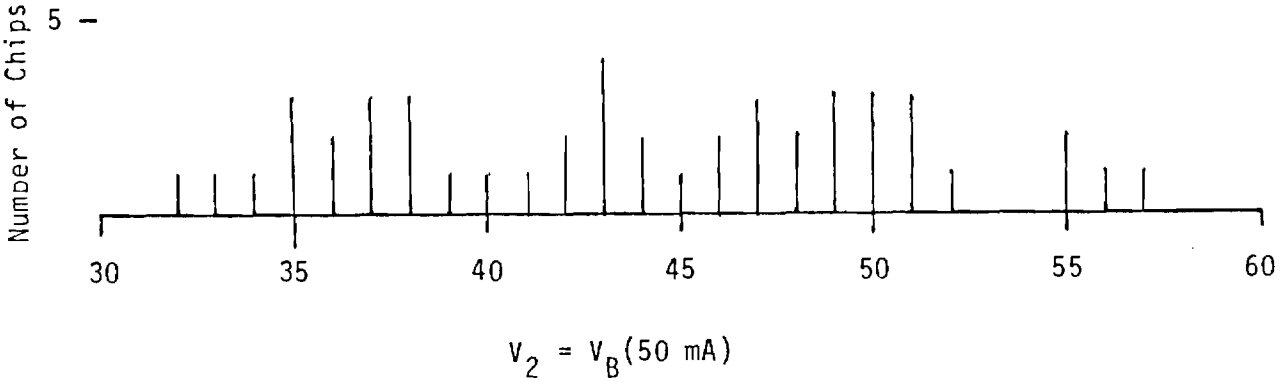


Figure 1. Preselection Data Summary,
Lot VSX9251AM, Chips 51-100





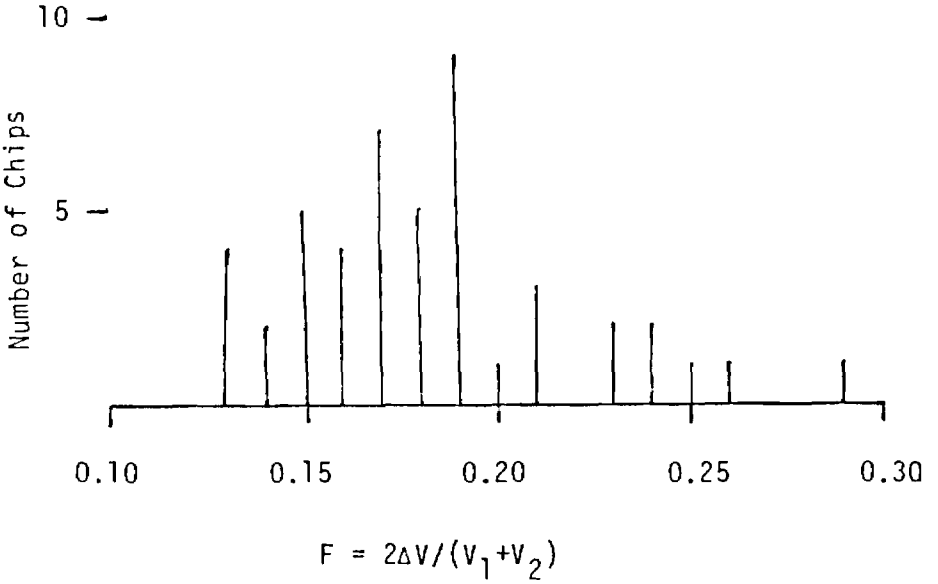


Figure 2. Preselection Data Summary, Lot VSX9251AM, Chips 1-50.

A-2351

Monthly Status Letter No. 8

Evaluation and Assembly of X-Band Pulsed GaAs IMPATT Diode Chips

P.O. No. P0163130

Contract period covered
11 October 1979 through 10 November 1979

A-2351

Submitted to

General Dynamics
Pomona Division
Pomona, California 91766

by

Solid State Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting through

Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

Prepared by

C.T. Rucker
W.K. Parks

26 November 1979

INTRODUCTION

Work done from October 11 through November 10, 1979 on the series connection of X-band IMPATT diodes (Lot No. VSX9251AM) is reported in this Status Letter. Possible thermal problems with AV174 packages were reported last month. During this report period, thermal measurements were made on two previously fabricated assemblies to determine their thermal resistance, θ_T. In particular, three measurements were made on two-chip assembly VSX9251AM-N when it was screwed into the 1/2 inch diameter puck (1) without heat sink grease, (2) with heat sink grease and (3) soldered into the puck. These measurements showed a twofold decrease in thermal resistance between the first and third case, but a much smaller decrease was observed between cases (2) and (3). RF tests were then repeated on the two-chip assembly after soldering, but power output and efficiency were less than previously measured. Although it was not expected, the performance dropoff may have been due to possible damage to the assembly during soldering.

DETAILED DISCUSSION, THERMAL RESISTANCE MEASUREMENT

A. Theory

The total thermal resistance of a diode, θ_T, is defined as the ratio of the incremental DC power dissipated in the diode. If the temperature reference is that of the puck (heat sink) into which the packaged diode is screwed, then θ_T includes the junction to package thermal resistance and the package-to-heat sink thermal resistance. This may be expressed as

$$\theta_T = \frac{T_j - T_s}{P_{diss}} \qquad (1)$$

where T_j = junction temperature,

T_s = heat sink temperature and

P_{diss} = power dissipated.

The most straightforward way to measure θ_T would be to apply known power to the diode, and measure T_j and T_s directly with thermocouples and/or infrared radiometers. This method is impractical for most purposes, however.

A more convenient method relies on the fact that the breakdown voltage, V_B, is a function of the junction temperature. Over the range of measurement interest (20 °C to 100 °C), the dependence is approximately linear with temperature. At higher temperatures, V_B is not usually a linear function of temperature. Therefore, a single unique thermal resistance value is not determinable. For our purposes (comparison), the maximum of 100 °C is sufficient.

Figure 1 gives the IV characteristics of a reverse biased IMPATT diode. The curves labeled "ISOTHERMAL" are those obtained at different ambient temperatures when the test voltage and current pulses are short compared to the thermal time constant of the diode, so that the pulse does not change the junction temperature. A pulse width of less than 1 μsec is typically required. The curve labeled "DC" adds the effect of the increase in breakdown voltage with temperature to the isothermal curves. It may be obtained by increasing the current from a DC supply to the diode in increments and taking the data point-by-point.

The voltage across the diode may be expressed as a function of the junction temperature (T_j) and current (I) in the following manner:

$$V(T_j,I) = V_B(T_j) + I\ R_{SC},$$

where R_{SC} = space charge resistance measured in the absence of thermal effects.

Expansion of $V_B(T_j)$ about T_o yields

$$V_B(T_j) = V_B(T_o) + \frac{\partial V_B}{\partial T}\Big|_{T_o} [T_j - T_o) + \cdots$$

or $$V_B(T_j) \cong V_B(T_o) + \beta\, V_B(T_o)\, [T_j - T_o]$$

where $$\beta = \frac{1}{V_B(T_o)} \frac{\partial V_B}{\partial T}\Big|_{T_o} .$$

The total voltage may then be expressed as

$$V(T_j,I) = V_B(T_o) + \beta\, V_B(T_o)\, [T_j - T_o] + I\, R_{SC} .$$

The power dissipated in the diode is given by

$$P_{diss} = I\, V(T_j,I) = I\, V_B(T_o) + I\, \beta\, V_B(T_o)\, [T_j - T_o] + I^2\, R_{SC}$$

or $$T_j - T_o = \frac{V(T_j,I) - V_B(T_o) - I\, R_{SC}}{\beta\, V_B(T_o)} .$$

Applying the definition of equation (1), one has:

$$\theta_T = \frac{V(T_j,I) - V_B(T_o) - I\, R_{SC}}{I\, \beta\, V(T_j,I)\, V_B(T_o)} . \qquad (2)$$

By directly measuring R_{SC} and β, which is an effective voltage-temperature calibration, one may obtain the thermal resistance. Early efforts took this direct approach[1,2]. The measurement procedure described below uses the method with slight modifications to ease computation of θ_T.

B. Measurement Procedure

Figure 2 shows the apparatus used to make thermal measurements. The DC power supply must be capable of supplying up to 150 mA of current at breakdown. The heater is a resistor anchored to a copper plate of approximate dimensions 2-1/2" x 2" x 3/16" which also has water cooling provisions. The packaged diodes were screwed into a threaded puck which was then clamped to the plate. A thermocouple was installed in the puck near the package. Pulse length and duty were set at 0.3 μsec and 0.05%, respectively, and maintained at those values for all measurements.

Step A of the measurement was a voltage temperature calibration. Water flow established both the heat sink (puck) and diode junction temperature at some initial reference temperature, T_o, after which coolant flow was stopped. Throughout Step A, the DC supply was adjusted to provide 1 mA bias current to maintain the device near breakdown. By superposition, it may be shown that the DC supply and pulser waveform combine to produce a composite waveform as shown in the lower left inset of Figure 2. The pulser was set to provide a 25 mA pulse.

---

1. R.H. Haitz, et al., "A Method for Heat Flow Resistance Measurements in Avalanche Diodes," IEEE Trans. Electron Devices, vol. ED- , pp. 438-444 May 1969.

2. "Pulse Measurements of Transient Thermal Response and Temperature of Avalanching p-n Junction," Electronics Letters, vol. 7, no. 17, p. 481, 26 August 1971.

The voltage increase, $V^{+}_{P_o}$, due to the current pulse when added to the bias voltage, $V_B(T_o)$ yielded the "isothermal" voltage corresponding to a 25 mA current level. Call this voltage $V_{iso}(T_o, 25\ mA)$. Next, the temperature was raised to T_1 by the auxiliary heater, then $V_{iso}(T_1, 25\ mA)$ was measured. This procedure was repeated to obtain $V_{iso}(T_i, 25\ mA)$ for several higher temperatures, T_i. When the voltage is plotted against temperature, one obtains the incremental change of the breakdown voltage, V_B, with temperature:

$$m_T \triangleq \frac{\Delta V_B}{\Delta T_A} = \frac{V_B(T_i) - V_B(T_o)}{T_i - T_o} = \frac{V_{iso}(T_i\ 25\ mA) - V_{iso}(T_o, 25\ mA)}{T_i - T_o}$$

where i = temperature index.

Note that m_T is constant for $T_j < 100$ °C because of the linear dependence of V_B on junction temperature.

In step B, the dependence of breakdown voltage on power dissipation was first obtained, then converted to the dependence of temperature difference on power which determined θ_T. The DC bias current was first set to 25 mA = I_{bias_o}, and the water used to set the heat sink temperature at T_{S_o}. Because of the high bias, the junction temperature was elevated to a temperature T_{j_o}, such that $T_{j_o} > T_{S_o}$. The dissipation, P_{diss_o}(25 mA) and DC voltage V_{ref_o} were then measured at the 25 mA level.

The bias current was increased to higher levels I_{bias_1}, ..., I_{bias_i}..., for which there were higher power dissipations P_{diss_1}, ..., P_{diss_i}, ... At these higher bias levels, a negative going current pulse was used to return the current to I_{bias_o} along an isothermal characteristic. The

magnitude of the voltage pulses corresponding to these current pulses was denoted by $V^{-}_{P_i}$. The voltages $V_{ref_i} \triangleq V_{bias_i} - V_{p_i}$, are the voltages of the T_{j_i} isothermal evaluated at a current level of I_{bias_o} = 25 mA. The difference in these voltages, $\Delta V_{ref_i} \triangleq V_{ref_i} - V_{ref_o}$, corresponded to the difference of the two junction temperatures. The junction temperature difference was calculated via the calibration of Step A.

$$\Delta T_{j_i} = T_{j_i} - T_{j_o} = \Delta V_{ref_i} \left(\frac{\Delta T_A}{\Delta V_B}\right)$$

Recall the definition of thermal resistance:

$$T_j - T_s = \theta_T \cdot P_{diss}$$

$$(T_{j_i} - T_{s_i}) - (T_{j_o} - T_{s_o}) = \theta_T (P_{diss_i} - P_{diss_o})$$

If the sink is held constant $T_{s_i} = T_{s_o}$, and

$$T = \frac{T_{j_i} - T_{j_1}}{P_{diss_i} - P_{diss_o}} = \frac{\Delta T_{j_i}}{\Delta P_{diss}} \quad .$$

If we define $m_p = \frac{\Delta V_{ref_i}}{\Delta P_{diss_i}}$, and note that m_p is a constant then

$$\theta_T = \frac{m_p}{m_T} \tag{3}$$

Equation (3) gives thermal resistance in terms of the quantities actually measured and plotted. Calculation of R_{SC} and β is possible from the data taken, but not necessary.

SYNOPSIS OF MEASUREMENT TECHNIQUE

Below 100 °C, batch VSX9251AM IMPATT diodes exhibit a breakdown voltage which is a linear and increasing function of temperature. The slope (m_t) of this function can be measured by heating the device to various temperatures and measuring the breakdown voltage V_B at some low pulsed current I, giving:

$$m_t = \frac{\Delta V_B}{\Delta T_j} \quad .$$

If one then applies significant bias power to the device (say by application of a DC current) the breakdown voltage will increase. If the power input is interrupted momentarily by an opposing pulse which returns the current to the value I, it is possible then to determine another linear function V(P) whose slope

$$m_p = \frac{\Delta V_B}{\Delta P}$$

provided that the interrupting pulse is short compared to thermal time constant of the diode (< 1 μsec).

The thermal resistance can then be readily determined as

$$\theta_T = \frac{m_p}{m_t}$$

THERMAL MEASUREMENT RESULTS

Measurements were made on two assemblies available from previous RF testing. VSX9251AM-A is a single-chip assembly mounted in a type N-33 micro-pill package. Heat sink grease was applied to the threads, and the package was then screwed into the puck. The data taken, along with that taken for the second diode, appear in Appendix I. A thermal resistance of θ_T = 17.2 °C/watt was calculated from the data for the first device.

Measurements were then made on the two-chip assembly, VSX9251AM-N, with the assembly screwed into the puck (1) with heat sink grease, (2) without heat sink grease and (3) soldered into the puck. The results are summarized as follows:

Assembly VSX9251AM-N

THERMAL MEASUREMENTS

Mounting to Puck	[V/°C] m_T	(V/watt] m_p	(°C/watt] θ_T
Without Heat Sink Grease	0.232	2.53	10.90
With Heat Sink Grease	0.232	1.67	7.20
Soldered	0.241	1.41	5.85

The assembly showed a decrease in θ_T of almost one-half ($\frac{10.9-5.85}{10.9} = 0.46$) when progressing from an assembly simply screwed into the puck without grease to the same assembly soldered into the puck, a surprisingly large change. The reduction in thermal resistance suggested that improved RF performance

might be forthcoming for the assembly soldered into the puck. The assembly was RF tested and the data compared with previous data for the same diode mounted in the puck with only heat sink grease.

RF Performance VSX9251AM-N

Mounted With Heat Sink Grease: 9/4/79

[volts] V	[Amps] I	[Watts] P	[Watts] P_o	[%] η	[GHz] f_o	[μsec] P.W.	[%] Duty
105.	0.80	84.0	16.7	19.9	9.7	1	20

Soldered Into Puck: 11/19/79

106.	0.90	95.4	13.7	14.3	9.7	1	20
100.	0.80	80.0	10.4	13.0	10.0	1	15
95.	0.70	66.5	7.5	11.3	10.2	1	10

The diode did not behave as expected. With decreased thermal resistance, higher efficiency and power output were expected from the soldered device. When poorer performance was observed at 20% duty cycle, the duty was dropped to 15%, then 10%, with even poorer results. The poorer results may be due to possible damage suffered by the diodes when they were soldered into the package. In retrospect, it is also possible that the dramatic decrease in thermal resistance may have been partially due to imperfections in the threaded puck. Although the assembly was screwed in tightly, the threads at the extreme surface of the puck in use have been enlarged during constant

use, and the fit between the shoulder of the package and puck may not have been as snug as it should have been for the trials with and without heat sink grease. When the assembly was soldered into the puck, the gaps, if indeed they existed, were filled with solder so that the problem was eliminated. Additional tests to verify the large change noted appears to be in order. Unfortunately, the project schedule and funding do not allow for additional work of this type. Therefore, effort will now concentrate on assembly and test of Phase III deliverable multichip diodes.

PLANS FOR NEXT MONTH

- Fabrication of three-chip package assemblies.

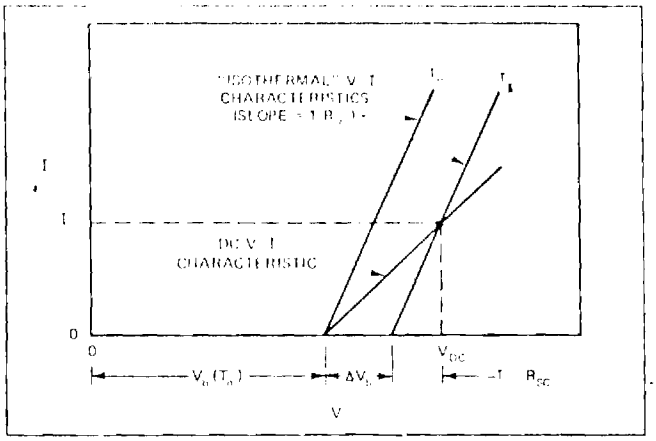
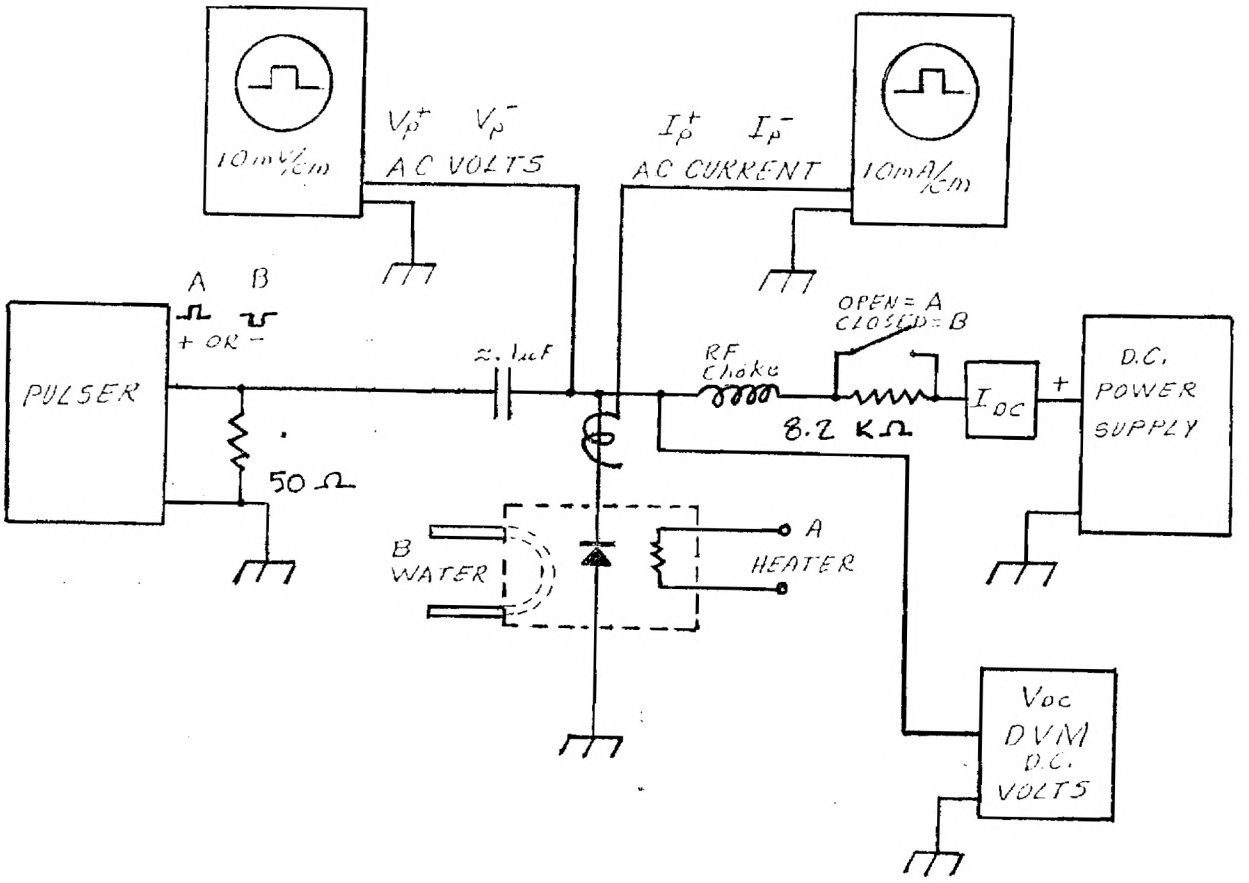


Figure 1. IV Characteristics of Reverse Biased IMPATT Diode



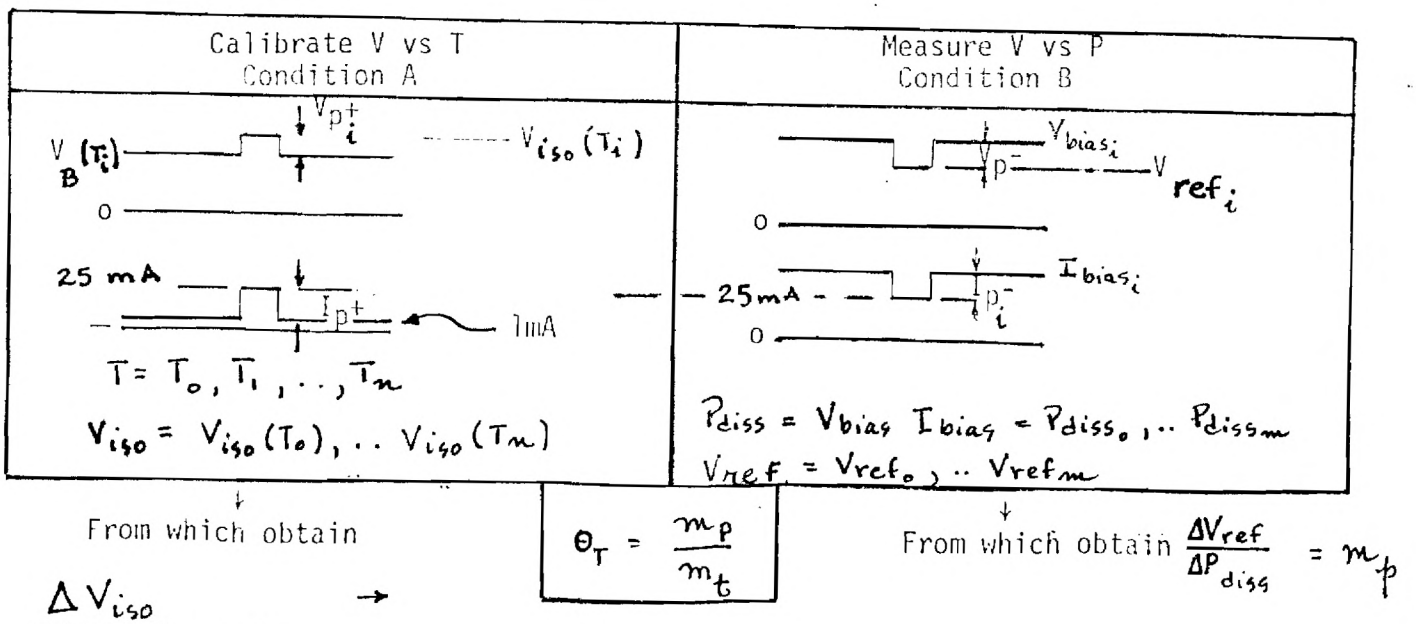


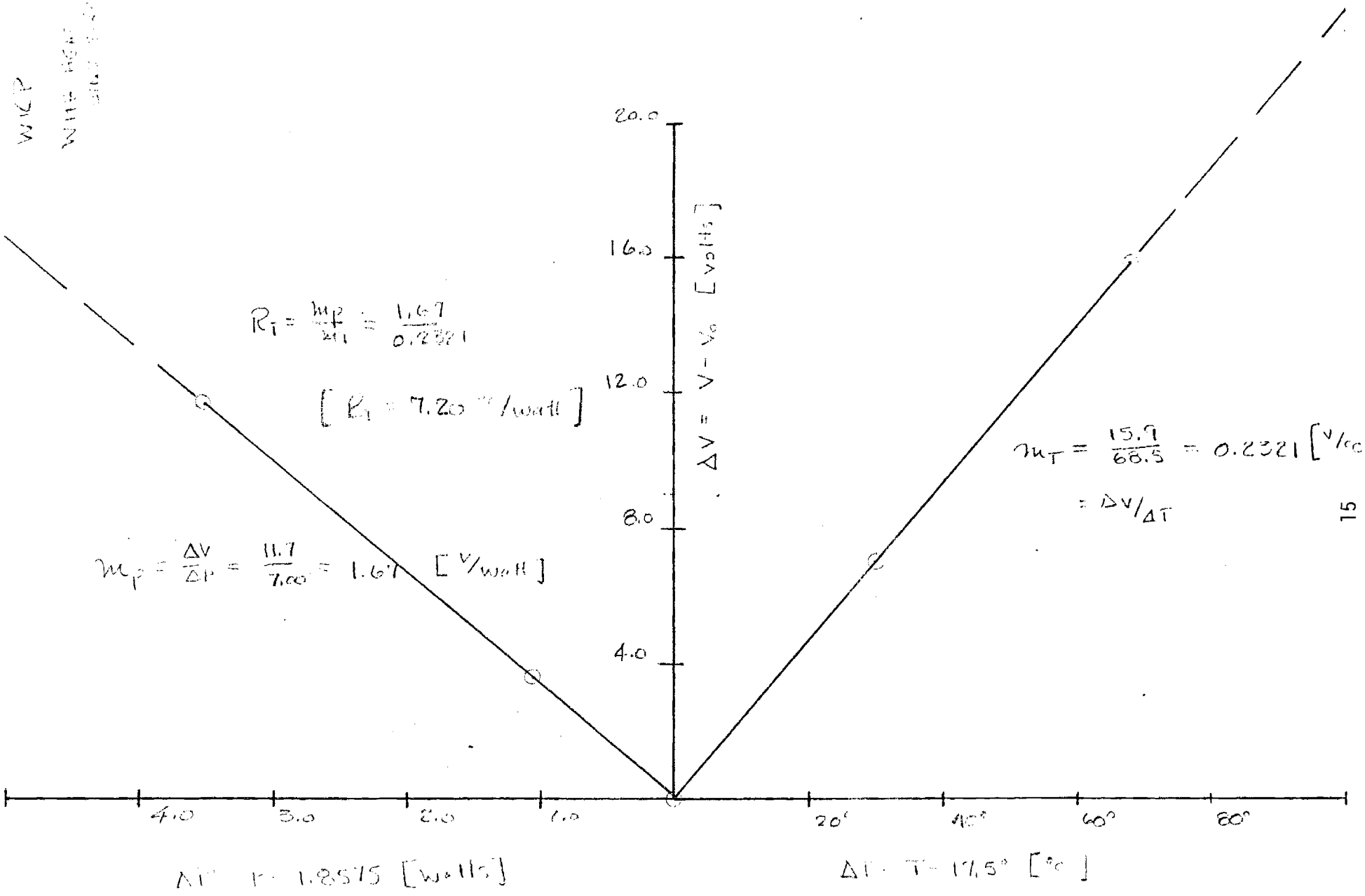
Fig. 2. Circuit and Test Conditions, Thermal Resistance.

APPENDIX

Thermal Resistance

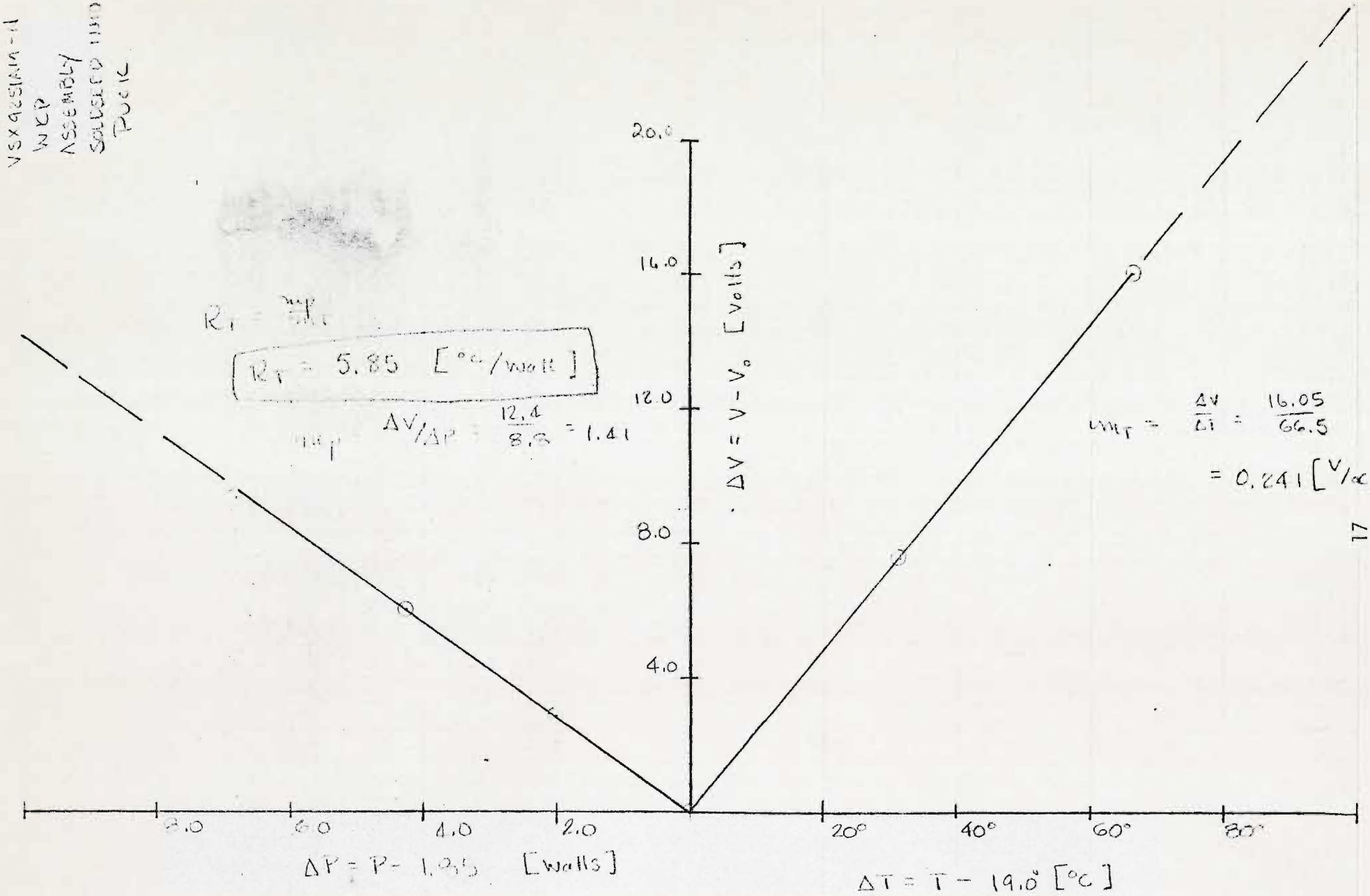
Measurement Data

WKP
(N-33,
Small Package)
ΔV = V − V₀ [Volt]
ΔT = T − T₀ [°C]
20°
40°
-20°


20.0
16.0
12.0
8.0
4.0
ΔV = V − V₀ [volts]
4.0
3.0
2.0
1.0
20°
40°
60°
80°
ΔT = T − 17.5° [°c]
ΔP = P − 1.8575 [watts]
$R_1 = \frac{m_p}{m_1} = \frac{1.67}{0.2321}$
[R₁ = 7.20 °/watt]
$m_p = \frac{\Delta V}{\Delta P} = \frac{11.7}{7.00} = 1.67$ [V/watt]
$m_T = \frac{15.9}{68.5} = 0.2321$ [V/°c]
$= \Delta V/\Delta T$

W.K.P
W/O HEAT
SINK GREASE
4.0
8.0
12.0
16.0
20.0
2.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
[V / mW]
0.232

VSX 4251AM-1
WCP
ASSEMBLY
SOLDERED 1183
PUCK



$R_T = \frac{\Delta T}{\Delta P}$

$R_T = 5.85$ [°C/watt]

$\Delta V/\Delta P = \frac{12.4}{8.8} = 1.41$

$m_T = \frac{\Delta V}{\Delta T} = \frac{16.05}{66.5}$

$= 0.241$ [V/°C]

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A-2351

Monthly Status Letter No. 9

Evaluation and Assembly of X-Band Pulsed GaAs IMPATT Diode Chips

P.O. No. P0163130

Contract period covered
11 November 1979 through 5 January 1980

A-2351

Submitted to

General Dynamics
Pomona Division
Pomona, California 91766

by

Solid State Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting through

Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

Prepared by

C.T. Rucker
W.K. Parks

5 January 1980

INTRODUCTION

Work done from November 11, through January 5, 1980, on the series connection of X-band IMPATT diodes (Lot No. VSX9251AM) is reported in this Status Letter. Effort has centered upon the construction of two- and three-chip assemblies to be delivered to General Dynamics at project completion.

FABRICATION

From the remaining diodes in the second batch of fifty received in September, several groups of two and three diodes were selected on the basis of their breakdown voltages, lack of premature breakdown, and low walkout characteristics. From these groups fabrication of seven packaged assemblies was begun. Included are three two-chip and four three-chip assemblies. The two-chip assemblies are complete and awaiting RF test. Of the four three-chip assemblies, the first developed irreversible premature breakdown and leakage during assembly and had to be abandoned. The remaining three three-chip assemblies are in the last stage of the fabrication. When they are complete, all six diodes will be RF tested and shipped to General Dynamics.

FUTURE PLANS

With the construction and test of these six assemblies, technical work on the project will be complete. The assemblies will be delivered to General Dynamics, and a complete report detailing the results of the program will be prepared.

A-2351

FINAL REPORT

PROJECT NO. A–2351

EVALUATION AND ASSEMBLY OF X–BAND PULSED GaAs IMPATT DIODE CHIPS

By

W. K. Parks and C. T. Rucker

Prepared for

GENERAL DYNAMICS
POMONA DIVISION
POMONA, CALIFORNIA 91766

For Period 28 February 1979 through 18 January 1980
P. O.: 163130

February 1980

GEORGIA INSTITUTE OF TECHNOLOGY

Engineering Experiment Station
Atlanta, Georgia 30332

1980

PREFACE

The work described herein was performed primarily in the Solid State Sciences Division of the Electromagnetics Laboratory, Engineering Experiment Station, Georgia Institute of Technology. The work was under the direction of C. T. Rucker; other principal Georgia Tech contributors were W. K. Parks, J. W. Amoss, H. M. Harris and G. N. Hill. Scanning Electron Micrography has played an important role in this work. We acknowledge the assistance of J. L. Hubbard of the Analytical Instrumentation Laboratory in this regard.

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SECTION I

INTRODUCTION

This report describes research performed over the period February 28, 1979, through January 18, 1980. Research effort centered about the fabrication and evaluation of series connected X-band pulsed GaAs IMPATT multichip assemblies. The project consisted of four phases or tasks:

I. Chip Evaluation

II. Package Feasibility and Development

III. Fabrication of Two-Chip Assemblies

IV. Technology Transfer

General Dynamics furnished one hundred chips obtained from Varian to Georgia Tech. These diodes were supplied in two batches of fifty each, but all were from the same lot. Chip evaluation showed a larger than usual proportion of the diodes exhibited premature breakdown. Initial RF evaluation showed that the RF power output and efficiency of the devices after assembly were also less than expected.

Because of the low power outputs observed, it was decided to construct some three-chip as well as two-chip assemblies. This dictated the use of the larger type AV174 ceramic microwave package, rather than the smaller N-33 originally proposed. A total of twenty-two assemblies were fabricated during the course of the project, but of these, only three multichip assemblies were deliverable to General Dynamics. Most of the rest failed in futile attempts to achieve reasonable power levels. In retrospect, it seems obvious that most of the difficulty in obtaining the power levels desired stemmed from the low power output of the individual chips. A possible heat sinking problem may be associated with the AV174 package, and is discussed herein.

Section II of the report deals with preliminary chip evaluation of Task I. Section III presents the multichip experiments, and constitutes the bulk of the effort on Tasks II and III. Section IV contains the thermal analysis portion of the failure analysis performed on the failed multichips. The various appendices contain a more theoretical discussion of thermal measurements than is presented in Section IV, as well as a thorough compilation of much of the data taken.

SECTION II

DIODE CHIPS

2.1 GENERAL

The diode chips used for this program came from Varian Lot No. VSX9251AM. The diodes were received in two batches of fifty each. The first fifty were received on March 28, 1979; the second on September 10, 1979. For each batch, the chips were received in five plastic containers, each of which contained ten chips. In order to identify the diodes, the vendor placed a small square of self adhering label material adjacent to the first and tenth chip positions in each container. Unfortunately, the squares were thick enough to raise the top lid of the container far enough away from the bottom to allow the chips to be jarred out of their specified slots. In this way, the chips were shifted throughout each of the ten separate containers. This completely scrambled the numbering/identification system supplied by the vendor.

Because all of the diodes had to be renumbered, direct comparision of data supplied by the vendor for each diode with that taken at Georgia Tech was not possible. Only comparisons based on averages within a given container were possible.

More serious, however, was the tenacious attachment of the chips to the adhesive on the labels. Removal of chips from the adhesive cannot be completely accomplished with solvents, and was not attempted. Instead, removal was done by means of a vacuum pickup and tweezers. This process was quite hazardous to the chips, and minor deformation of some of the heat sinks was unavoidable. Possible contamination of some of the chips may also have occurred. Even so, no fatal damage to any of the chips was observed.

2.2 CHIP PRESELECTION AND EVALUATION

The two batches of fifty diodes were subjected to a stringent preselection procedure designed to eliminate weak chips and indicate possible problems, if any, in those remaining. This procedure was developed and refined in several previous chip combining programs.

First, several chips were placed in prepositioned indentations on a polished nickel plated copper block. The block is shown in the inset of Figure 1. The block was placed on the foot plate of the test fixture (Figure 1). The chip was then raised into contact with an insulated pressure stylus which was connected to a curve tracer. A pressure of about 300 Kg/cm^2 was used to insure adequate thermal contact between the diode and copper block.

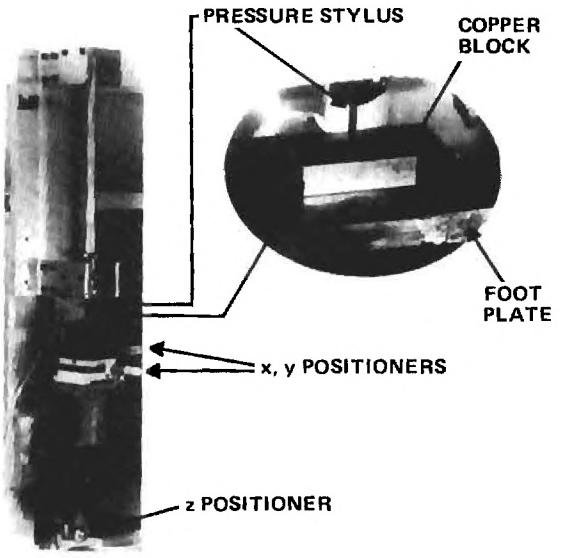


Figure 1. Preselection Test Fixture

For each chip, a current in excess of 100 mA was applied to stress the device. The I-V characteristic curves corresponding to applied currents of 1 mA and 50 mA were photographed. The photographs were then used in the evaluation of the lot.

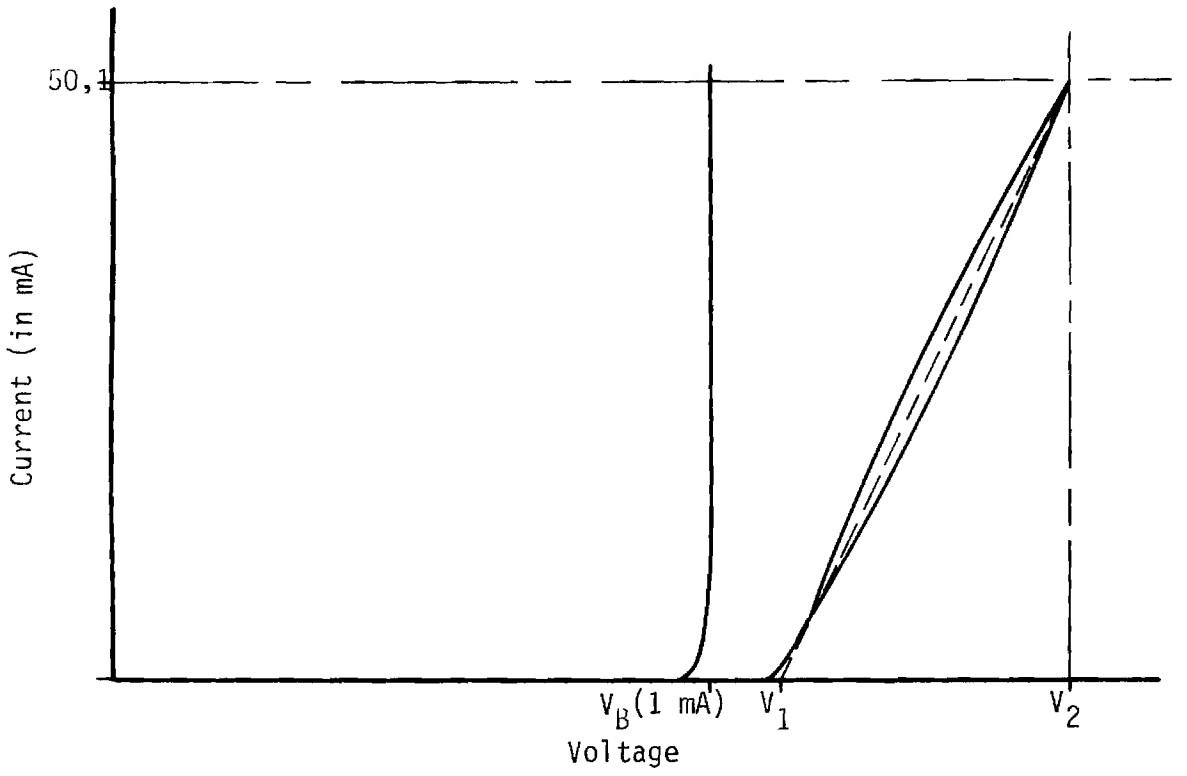


Figure 2. Definition of Preselection Parameters

Figure 2 is a sketch of a typical I-V characteristic. The parameters are defined as follows:

V_B(1 mA): the breakdown voltage measured at a current of 1 mA. This current is usually sufficient to prevent erroneous V_B readings which sometime result from premature breakdown and leakage.

$V_1 = V_B(\text{intercept})$: the V axis intercept of a line drawn through the high current hysteresis loop.

$V_2 = V_B(50\ \text{mA})$: the breakdown voltage measured at a current of 50 mA. This stress level is usually sufficient to establish the rate of change in V_B due to current and associated heating.

$F = \dfrac{2(V_2 - V_1)}{V_1 + V_2}$: an arbitrary slope parameter defined as the change in V_B (ΔV) normalized to the average of V_2 and V_1. It is a merit factor of sorts.

A listing of the values measured for these parameters appears in Table 1. For chips #1 through #50, the junction capacitance was measured at a reverse bias of 20.0 volts after completion of the preselection test. The capacitance data are presented in the last column of Table 1. Although the standard practice at Georgia Tech is to measure the capacitance at a voltage level just below breakdown, twenty volts was chosen to allow comparison with capacitance measurements made by the vendor. The preselection data are summarized graphically in Figures 3 and 4.

Figure 5 shows the discrepancy between the measurements made by Varian and Tech. Because the diodes were renumbered after they were scrambled during shipping, comparison diode by diode was not possible. However, average values for each box of ten diodes were computed and compared with the Varian average capacitance for the same box. For all five boxes, the Tech measurements were lower. The measurements were rechecked, but the reason for the discrepancy could not be ascertained.

From the preselection data of the first batch of fifty diodes, fifteen were chosen for Scanning Electron Microscope (SEM) analysis. Five were chosen because they exhibited nominally good I-V curves; ten because their curves contained various abnormalities. No initial SEM analysis following preselection was done on the second batch of fifty. However, after several

CHIP NO.	V_B(1mA)	V_1 V(Intercept)	V_2 V_B(50 mA)	ΔV (V_2-V_1)	F $(\frac{2\Delta V}{V_1+V_2})$	$C_j(\simeq V_B)$
1	30.0	31.0	35.5	4.5	0.14	**
2	28.5	29.5	35.0	5.5	0.17	**
3	27.5	28.5	32.5	4.0	0.25	4.82
4	38.5	40.5	49.0	8.9	0.19	3.78
5	35.0	36.0	42.0	6.0	0.15	4.71
6	34.5	36.5	42.0	5.5	0.14	4.08
7	36.0	38.0	47.0	9.0	0.21	4.33
8	37.0	41.0	50.0	9.0	0.20	4.45
9	35.0	36.0	41.0	5.0	0.13	4.12
10	40.0	41.0	49.0	8.0	0.18	4.37
11	39.5	41.5	50.0	8.5	0.19	3.66
12	37.5	38.0	46.0	8.0	0.19	4.57
13	40.0	43.0	55.0	12.0	0.24	3.58
14	34.5	36.0	44.5	8.5	0.21	3.65
15	36.0	37.5	44.5	7.0	0.17	4.48
16	33.5	34.0	39.5	5.5	0.15	4.53
17	33.0	34.0	40.0	6.0	0.16	3.89
18	31.0	37.0	48.0	11.0	0.26	4.65
19	32.0	36.0	43.0	7.0	0.18	4.32
20	29.5	30.5	36.0	5.5	0.17	5.06
21	31.5	33.0	38.5	5.5	0.15	4.97
22	27.5	28.5	33.5	5.0	0.16	5.40
23	30.5	32.0	36.5	4.5	0.13	4.81
24	37.0	38.0	45.5	7.5	0.18	4.03
25	32.0	41.0	52.0	11.0	0.24	3.57
26	*	--	--	--	--	--
27	43.5	43.0	51.0	8.0	0.17	3.89
28	38.5	39.0	47.0	8.0	0.19	4.37
29	28.0	29.5	37.0	7.5	0.23	4.69
30	37.0	38.0	46.0	8.0	0.19	4.31
31	*	--	--	--	--	3.87
32	36.0	37.0	43.5	6.5	0.16	5.04
33	44.0	45.0	55.5	10.5	0.21	4.06
34	33.5	36.5	43.5	7.0	0.18	4.55
35	29.0	30.0	35.0	5.0	0.15	4.39
36	29.0	29.5	37.0	7.5	0.23	4.29
37	31.0	33.0	37.5	4.5	0.13	4.81
38	31.5	32.5	38.0	5.5	0.16	4.07
39	41.0	43.0	51.0	8.0	0.17	3.93
40	40.5	50.0	57.0	7.0	0.13	4.14
41	22.5	46.5	56.0	9.5	0.19	3.80
42	37.0	41.0	49.5	8.5	0.19	4.11
43	39.0	40.0	47.5	7.5	0.17	4.28
44	36.0	38.0	51.0	13.0	0.29	3.19
45	41.0	43.0	50.0	7.0	0.15	3.93
46	*	--	--	--	--	3.55
47	35.5	36.0	43.0	7.0	0.18	4.31
48	31.0	31.5	38.0	6.5	0.19	5.05
49	27.5	29.0	34.5	5.5	0.17	4.16
50	39.0	39.5	48.0	8.5	0.19	4.47

CHIP NO.	V_B(1mA)	V_1 V(Intercept)	V_2 V_B(50mA)	ΔV (V_2-V_1)	F $(\frac{2\Delta V}{V_1+V_2})$
51	29.5	31.5	36.5	5.0	0.147
52	38.0	39.0	47.0	8.0	0.186
53	34.5	36.5	46.0	9.5	0.230
54	42.0	44.0	53.0	9.0	0.186
55	34.5	41.0	50.0	9.0	0.198
56	▲				
57	31.0	32.5	37.0	4.5	0.129
58	38.5	37.5	48.5	11.0	0.256
59	*				
60	30.0	31.0	39.0	8.0	0.229
61	37.5	38.5	46.0	7.5	0.178
62	29.5	31.5	40.0	8.5	0.238
63	32.5	34.0	40.0	6.0	0.162
64	37.0	41.0	51.0	10.0	0.217
65	39.5	41.5	50.0	8.5	0.186
66	34.5	36.0	42.5	6.5	0.166
67	29.0	31.0	35.5	4.5	0.135
68	32.0	33.0	39.0	6.0	0.167
69	39.5	41.0	48.5	7.5	0.168
70	32.0	33.0	38.5	5.5	0.154
71	30.0	31.5	36.0	4.5	0.133
72	35.5	37.0	42.5	5.5	0.138
73	30.0	33.5	39.0	5.5	0.152
74	31.0	32.0	37.5	5.5	0.158
75	35.0	36.5	44.0	7.5	0.186
76	34.5	35.5	42.5	7.0	0.179
77	31.5	38.5	46.5	8.0	0.188
78	35.0	35.5	41.5	6.0	0.156
79	35.6	36.5	43.5	7.0	0.175
80	●				
81	35.5	36.0	42.0	6.0	0.154
82	28.5	29.5	34.0	4.5	0.142
83	35.5	36.5	42.0	5.5	0.140
84	31.0	36.0	43.0	7.0	0.177
85	35.5	36.5	43.5	7.0	0.175
86	35.0	36.0	41.5	5.5	0.142
87	34.0	35.5	41.5	6.0	0.156
88	28.0	29.0	33.0	4.0	0.129
89	*				
90	40.0	41.5	50.0	8.5	0.186
91	42.5	43.5	52.0	8.5	0.178
92	37.0	37.5	44.5	7.0	0.171
93	36.0	37.5	44.0	6.5	0.160
94	*				
95	*				
96	37.0	39.0	39.0	7.0	0.165
97	42.5	42.5	42.5	8.0	0.167
98	37.5	38.0	38.0	6.0	0.146
99	39.5	41.0	41.0	8.0	0.178
100	34.5	36.0	36.0	7.5	0.189

* Diode failed during high current preselection test.

** Packaged before capacitance was measured.

▲ Diode failed during high current preselection test.

* Diode indicated short before current applied in preselection test.

● Diode lost during shipment.

Table 1. Preselection Data Summary: VSX9251AM, 1-100.

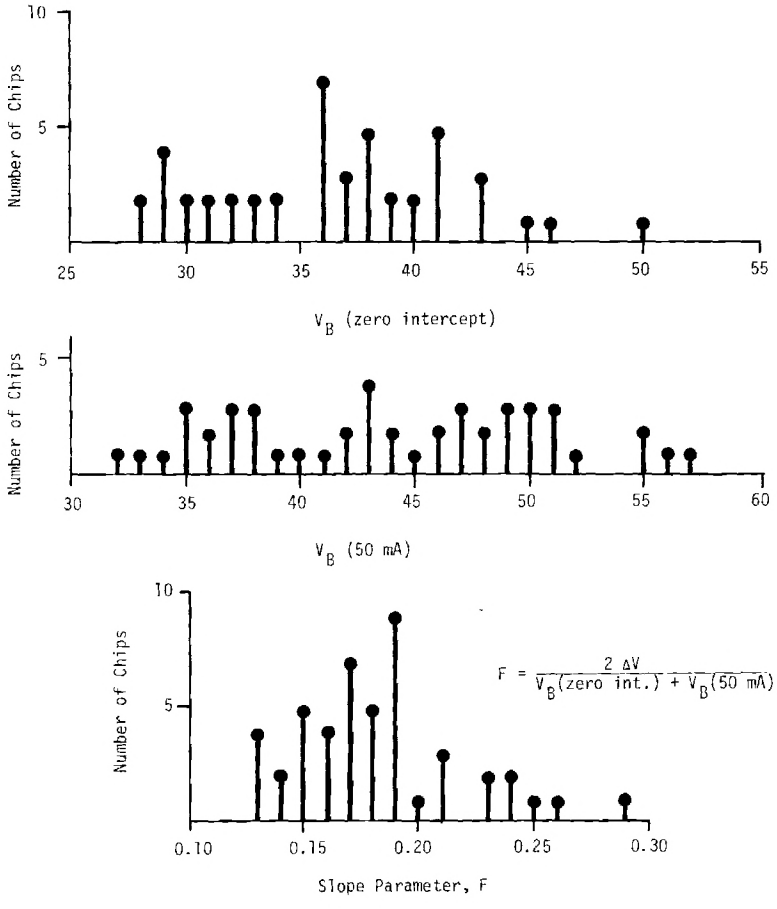


Figure 3. Preselection Data Summary, Lot VSX9251AM, Chips 1-50

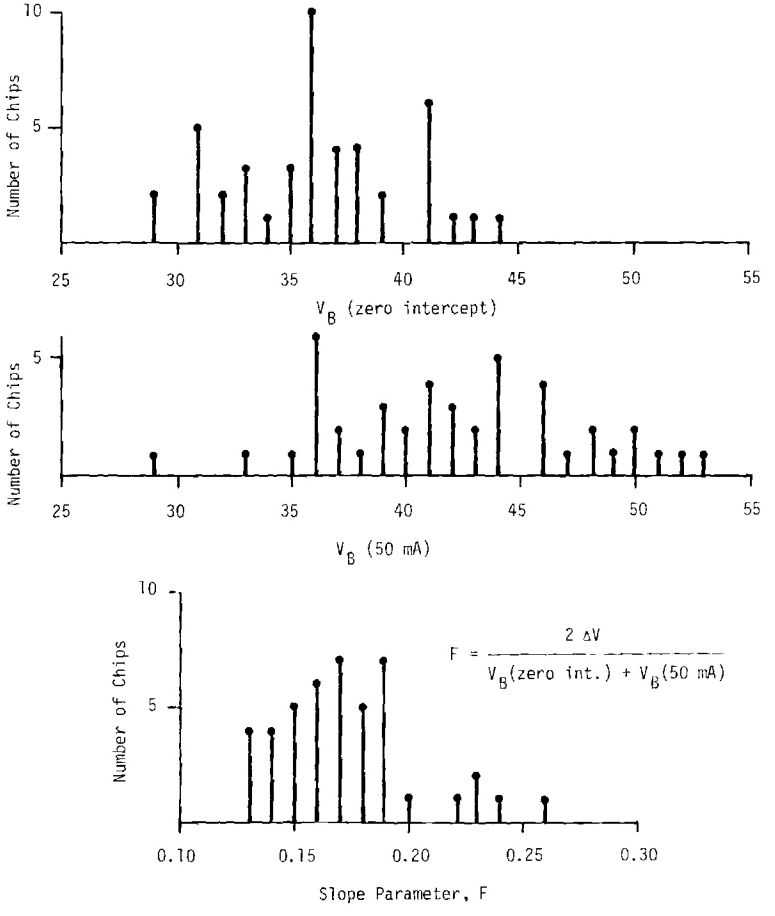


Figure 4. Preselection Data Summary, Lot VSX9251AM, Chips 51-100

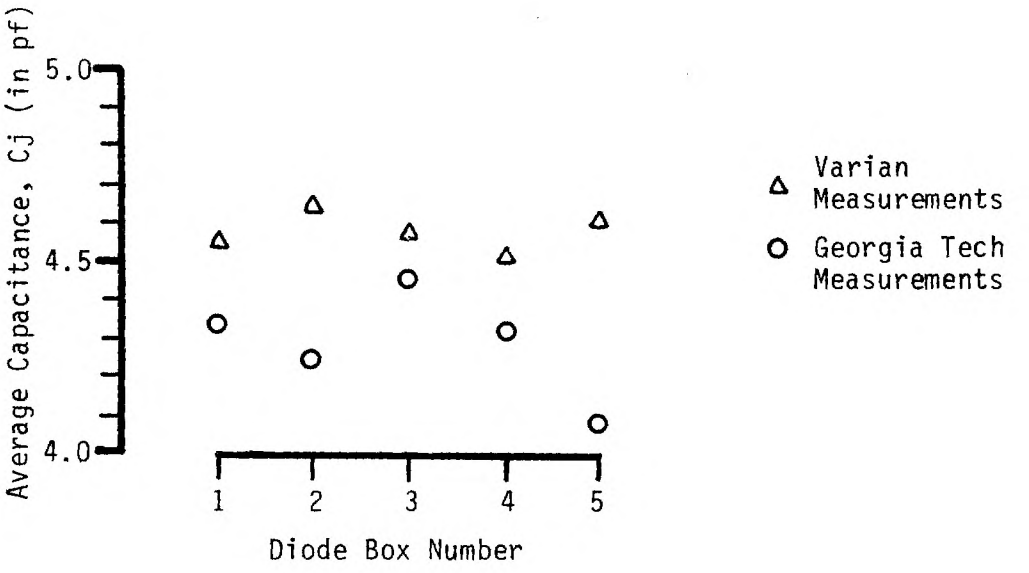


Figure 5. Comparison of Capacitance Measurements, C_j(20v), Taken by Varian and Georgia Tech.

multichip assemblies had been constructed from the second batch, twelve of the remaining unused chips were subjected to SEM analysis to insure that they possessed no peculiarities, not present in the first batch, which would cause the multichips to fail under RF testing.

Figure 6 is an SEM photograph of chip #1. The diode I-V curve exhibited a moderately sharp breakdown and little walkout of the breakdown voltage at high current. The figure shows that the diode possesses an excellent nominal geometry. Figures 7 and 8 are photographs of chips #19 and #69, and are two of the worst examples of variance from the nominal geometry. Chip #19 had an excessive amount of premature breakdown in its I-V characteristic, but #69 had a sharp breakdown. Deviation from circular geometry has not been known to contribute to premature breakdown previously. However, geometric defects, like the one in the center of the interface of chip #19 are often associated with contamination, which in turn is often the cause

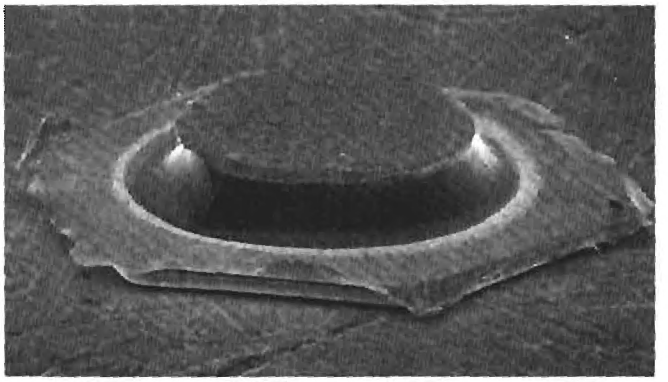


Figure 6. Chip (VSX9251AM, #1) Mag. = 143x. Typical Diode Showing Excellent Nominal Geometry.

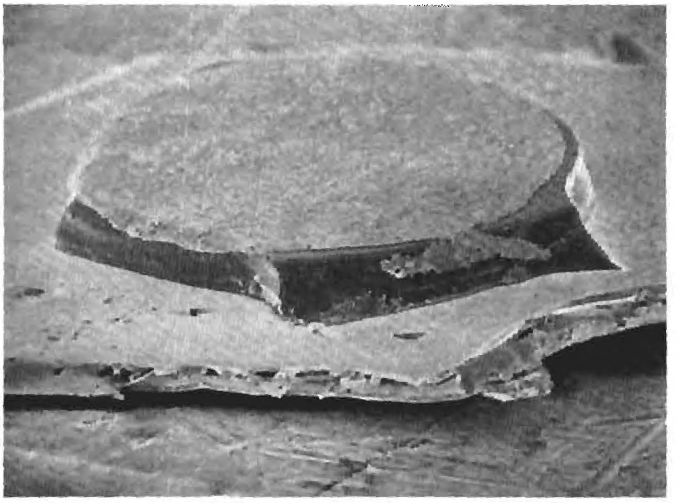


Figure 7. Chip (VSX9251AM, #19) Mag. = 238x. Diode With Noncircular Mesa Geometry.

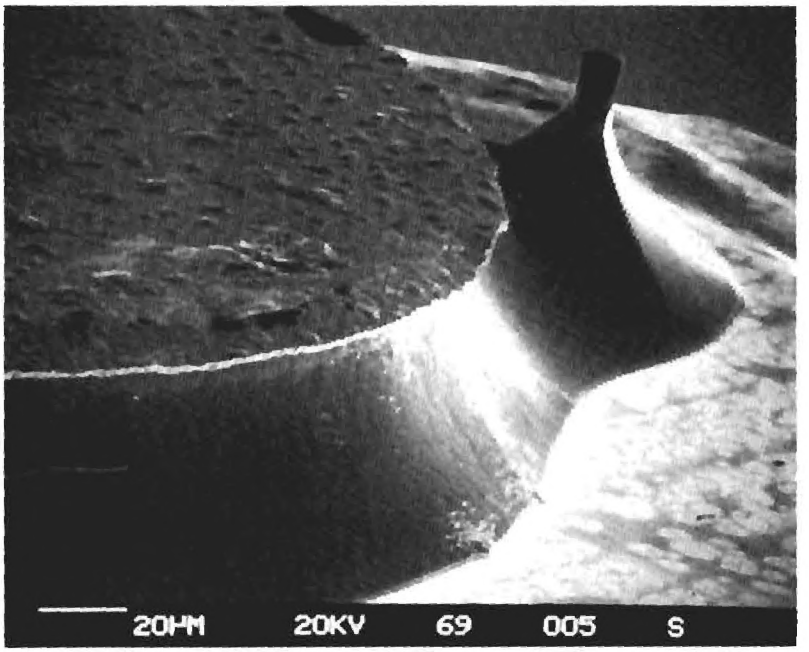


Figure 8.
Chip (VSX9251AM, #69) Mag. = 700x. Diode With Noncircular Mesa Geometry.

of premature breakdown. An example of this is chip #26 which failed during the high current stress phase of preselection. Figure 9 shows that the burnout occurred at the site of a geometrical defect.

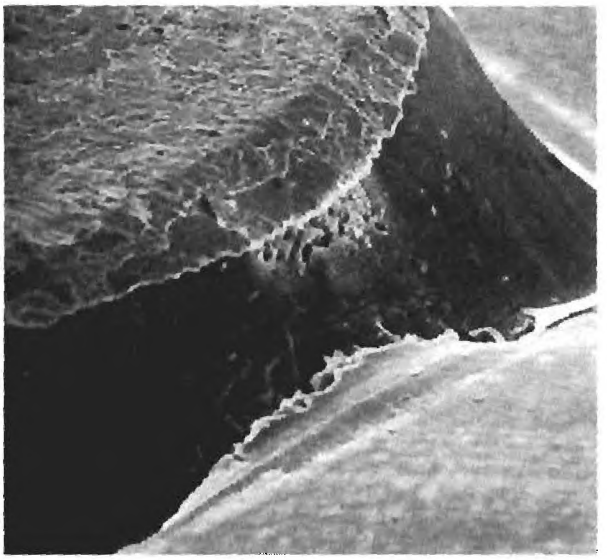


Figure 9. Chip (VSX9251AM, #26) Mag. = 700x. Failed Diode Showing Geometrical Defect at Mesa-Sink Interface.

Chip #41 suffered from excessive walkout of V_B at high current. The SEM (Figure 10) shows the diode had poor back contact metallization, which may have contributed to the thermal problem causing the walkout. Inadequate metallization may also cause additional problems during multipchip fabrication. Figure 11 shows chip #75 after being etched. The poor back contact allowed deep pits to be etched into the semiconductor. The chip began showing excessive premature breakdown during the etch stage, and had to be abandoned.

2.3 SINGLE CHIP RF EVALUATION

A block diagram of the setup used to test the RF performance of the completed single and multichip assemblies is presented in Figure 12. The combination of the high voltage supply, low voltage control supply, pulse

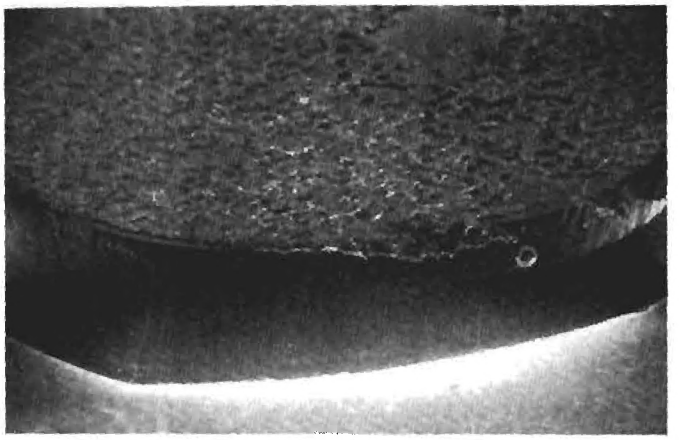


Figure 10. Chip (VSX9251AM, #41) Mag. = 357x. Diode With Excessive Walkout Showing Poor Back Contact Metallization.

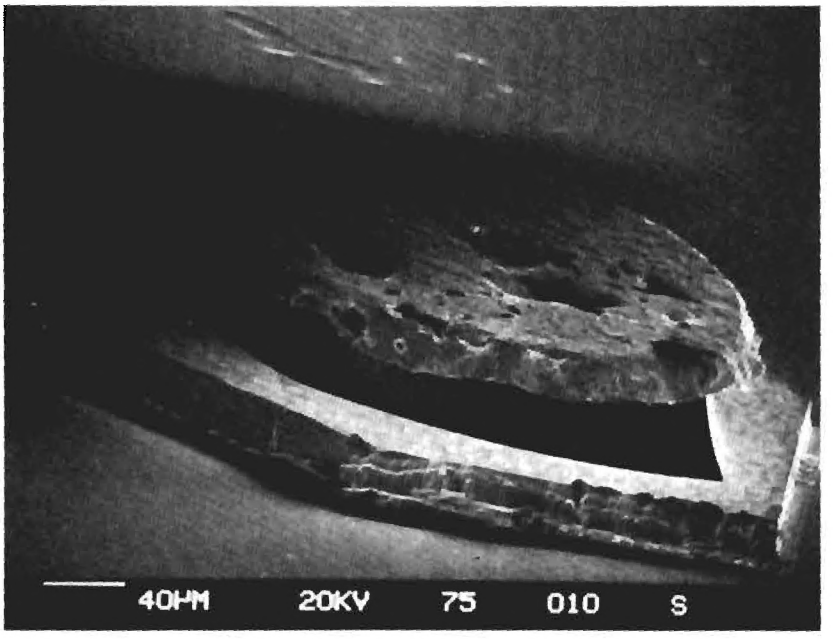


Figure 11. Chip (VSX9251AM, #75) Mag. = 275x. Diode With Pits After Etching Due to Poor Back Contact Metallization.

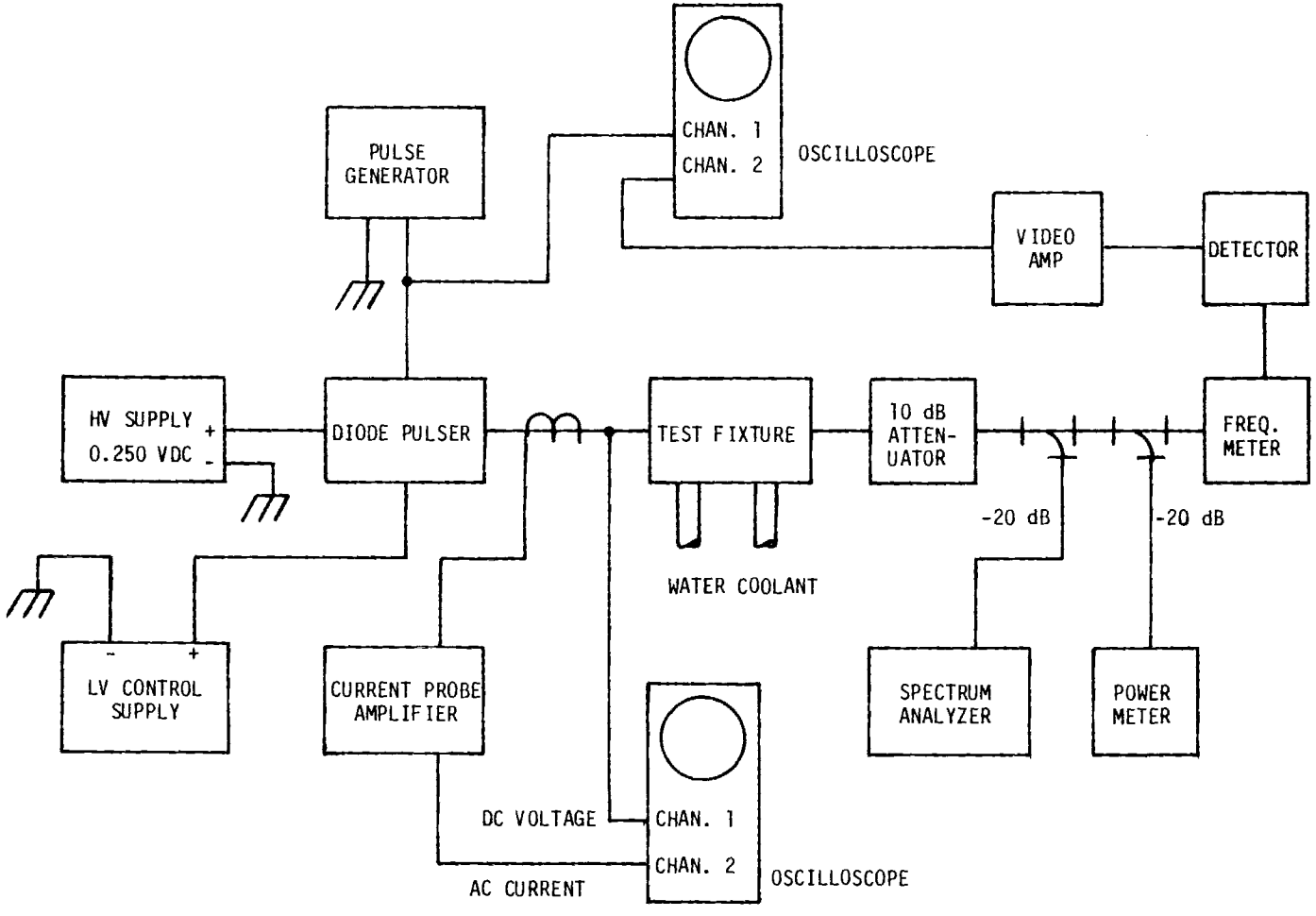


Figure 12. RF Test Setup Block Diagram

generator, and diode pulser allows a train of voltage pulses, with magnitude continuously variable from 0 to 250 volts, to be supplied to the test fixture. The pulse generator is used to control the width and duty cycle of the pulses; the low voltage supply controls the magnitude of the pulse up to the limit set by the high voltage supply.

The test fixture was described in detail by the sketches supplied with Monthly Status Letter No. 3. It has provision for water cooling the device under test, and has both an adjustable short circuit and a slide screw tuner for circuit tuning. Additional matching is provided by interchangeable transformers and top hats, and a bias ferrule which slides up and down the center conductor. The fixture accepts diode slugs of one-half inch diameter or less—assemblies may be fabricated directly on a slug, or built in packages which can then be screwed into the diode slug.

The rest of the equipment shown in the block diagram allow measurement of the input and output power of the device, operating frequency and frequency spectrum shape.

Data supplied by the vendor indicated that ten single chips from Lot No. VSX9251AM had been mounted in type N-57 packages and RF tested. The diodes averaged an output power of 18.2 W each with an average efficiency of 25.6%.

From the first batch of fifty, diode #2 was mounted in an N-33 package and designated assembly VSX9251AM-A. Diodes #1 and #3 were mounted in N-57 packages and designated VSX9251AM-B and -C, respectively. The RF data recorded for these three single chip assemblies are presented in Table 2 of Section III. The average output power per chip was 10.5 W at an average conversion efficiency of 14.9%—a poor showing in comparison with the vendor supplied data. The test setup was thorougly checked and recalibrated, and the data retaken with insignificant change in the results. An attempt was

made to obtain the ten packaged diodes tested by the vendor, so that a direct comparison could be made with the three diodes packaged at Georgia Tech using the same test fixture and measurement technique. The diodes, however, could not be found, and the only conclusion to be drawn from the preliminary RF evaluation was that the chips were only capable of producing relatively low power at reduced efficiency.

SECTION III.

MULTIPCHIP ASSEMBLIES

3.1 GENERAL

In programs prior to the present one, Georgia Tech demonstrated successful unpackaged, series connected multipchip assemblies containing as many as four Varian p^+-hi-lo chips, each chip capable of about 15 W peak power output. One vendor, Microwave Associates, had demonstrated a few successful experimental two-chip devices in AV174 ceramic packages.

The initial intent of General Dynamics' task was to determine the feasibility of packaged two-chip devices using chips from Varian Lot No. VSX9251AM supplied by General Dynamics. In view of the relatively low power and efficiency obtained with these chips in the preliminary RF evaluation (reference Section 2.3) it was decided that a portion of the task would be devoted to the fabrication of three-chip assemblies in the AV174 package.

In general, the feasibility of both two and three-chip packaged devices has been established, but few of the multichip assemblies have survived final testing. A more detailed discussion of the problems encountered is included in this section.

3.2 FABRICATION

The multichip assemblies produced in this program consisted of either two or three chips connected in series. In parallel with each chip was a capacitor whose purpose was to suppress low frequency parasitic oscillations which degrade the RF performance of an assembly. Although some of the first devices were assembled on one-half inch diameter diode slugs, the majority were built in ceramic microwave packages.

The diode chips used in the assemblies were matched for breakdown voltage at 1 mA, V_B(1 mA), and the slope of the high current I-V characteristic as measured by the quantity $\Delta V = V_B(50\ mA) - V_B(intercept)$ (reference Section 2.2). Diodes with poor I-V characteristics, e.g., those with excessive values of premature breakdown or thermally induced hysteresis in the high current curve, were not used in the assemblies. Capacitor values on the order of 1.0 pf were used in both two and three-chip assemblies. This value was determined empirically in past X-band power combining work, and represents a design tradeoff. Although a larger value might better reduce parasitics, it would lower the maximum operating frequency attainable by the assembly.

SEM photos appearing in Figures 13 and 14 give the general layout of a typical three-chip packaged assembly. The diamond on which the diodes and capacitors were mounted was 1.0 x 1.0 x 0.5 mm for two-chip assemblies and 1.5 x 1.0 x 0.5 mm for the three-chip ones. The diamonds were first cleaned, then a 200-300 Å layer of chromium was sputtered on. This was followed by a 2000 Å layer of gold sputtered on, and a 3 μm gold layer plated on. The device mounting pads and one side of the diamond were masked with black wax, and the rest of the metal film etched away using aqua regia and commercially available gold and chrome etch solutions. The diamond was then mounted in the base of the package using a thermal compression (TC) type bonder set at 300 °C and enough pressure to cause the diamond to sink slightly into the base.

The chips were selected and etched to the same junction capacitance using a 1:1:1 solution of methanol, hydrogen peroxide, and phosphoric acid. The heat sinks were trimmed with a razor blade to fit the mounting pads on

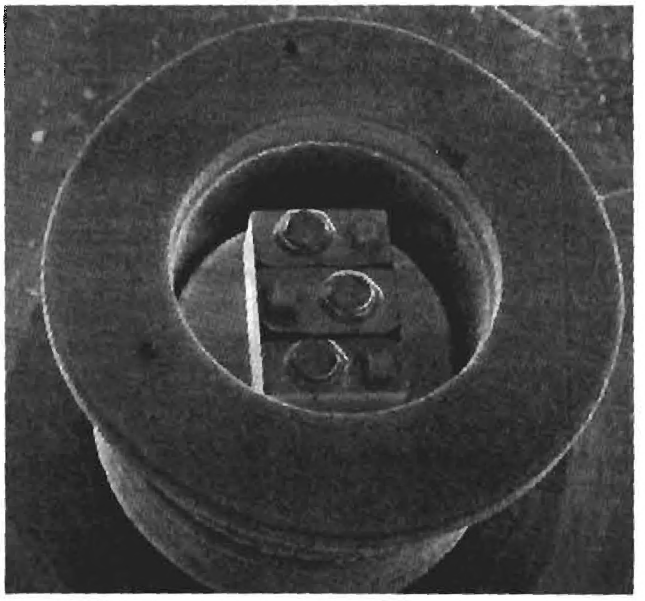


Figure 13. Three-Chip Assembly VSX9251AM-0. Nominal Geometry of Three-Chip Device Before Ribbons Attached. Mag. = 16X.

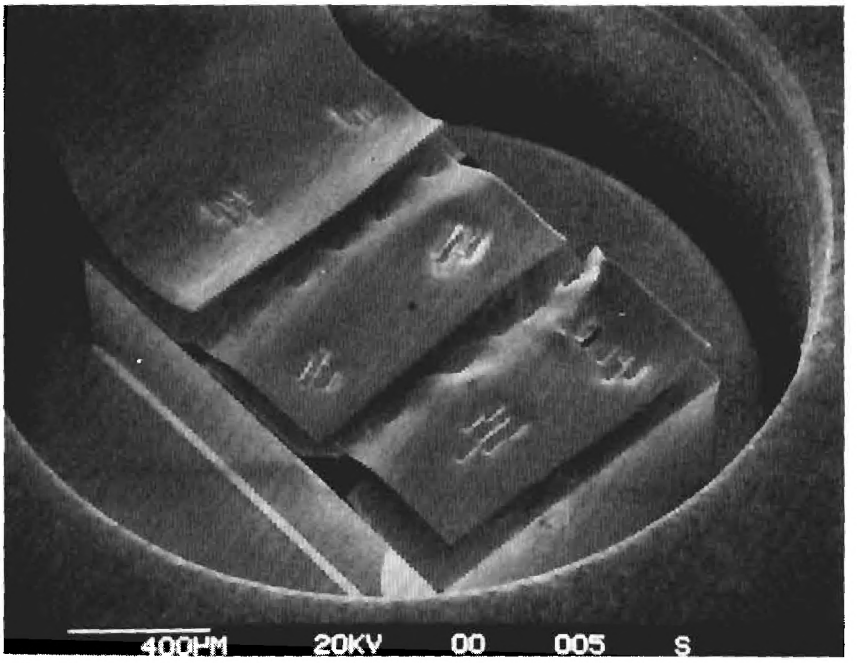


Figure 14. Three-Chip Assembly VSX9251AM-0. Nominal Geometry of Three-Chip Device. Mag. = 48X.

the diamond. The capacitors were TC bonded to the pads. The diodes were then attached to the pads using gold-tin alloy solder and an RF induction heating apparatus. Gold ribbons were trimmed to size and used to connect the diode-capacitor combinations in series. The ribbons were TC bonded to the components and the package.

From the 100 chips supplied, a total of 22 assemblies were fabricated, including the three single chip assemblies used in the preliminary RF evaluation. The assemblies fabricated may be categorized as follows:

Number of Assemblies	Type of Assembly	Package
3	1x1	N-33,N-57
7	1x2	None
6	1x2	AV174
1	1x3	None
5	1x3	AV174

3.3 RF TESTING AND FAILURE ANALYSIS

The same RF testing setup used in the preliminary evaluation of the single chips was used in the multichip evaluation. At the same time the three single chips were packaged, a three-chip unpackaged assembly was assembled on a one-half inch diameter diode slug and designated VSX9251AM-D. The data for the RF test of the assembly was summarized in Table 2, as is all the data from the testing of the 22 assemblies. VSX9251AM-D produced 33.5 w output at 14.3% efficiency, for an average of 11.2 w per chip. The three single chip assemblies A, B, and C, averaged 10.5 W at 14.9% efficiency. Although the overall power and efficiency figures are low, the realization of three times the average output power for a single chip from a three-chip assembly is encouraging.

DIODE LOT VSX9251AM RF TEST SUMMARY

Assy. #	Type	Pkg.	[Volt] V_B(1mA)	[pf] $C_T(V_B-1)$	[Volt] V	[Amp] I	[Watt] P	[Watt] P_o	[%] η	[GHz] f_o	[μsec] P.W.	[%] Duty
A	1x1	N-33	29	5.24*	51.0	1.20	61.2	9.1	14.9	9.2	1	20
B	1x1	N-57	31	5.55*	52.1	1.52	79.2	12.9	16.2	10.4	1	20
		Diode failed when it dropped mode. *C_T measured at 20.0 volts.										
C	1x1	N-57	27	3.62	45.0	1.55	69.8	9.5	13.7	10.5	1	20
D	1x1	No	102	1.50	146	1.60	234	33.5	14.3	10.2	1	20
		One diode failed when assembly dropped mode. It was converted to 1x2 and following data taken.										
D	1x2	No	-	-	110	1.53	168	17.1	10.2	9.7	1	20
E	1x2	No	54	2.40	One diode failed when diamond lifted off puck at a current of about 0.6 Amp.							
F	1x2	No	54	2.31	98.0	1.50	147	19.7	13.4	11.1	1	20
		One diode failed when the assembly dropped mode.										
G	1x2	No	55	2.36	One diode failed due to a coolant leak within the test fixture.							
H	1x2	No	72	2.20	100	1.00	100	14.0	14.0	10.0	1	20
	One diode failed when assembly dropped mode.											
I	1x2	No	72	1.70	112	1.00	112	16.0	14.3	10.5	1	20
	These RF operating values were measured subsequent to failure and re-etch after initial device failure.											
J	1x2	No	64	2.11*	96.0	1.30	125	17.3	13.8	10.3	1	20
	*C_T measured at 56.0 volts.											
K	1x2	No	78	2.13	107	1.30	139	24.1	17.3	9.9	1	20
L	1x2	AV174	-	One diode failed at low current (~ 0.4 Amp), before RF output was achieved.								
M	1x2	AV174	-	-	One diode failed at low current (~ 0.25 Amp), before small RF output could be recorded.							
N	1x2	AV174	68	-	104	0.75	78.0	15.4	19.7	9.73	1	20
O	1x3	AV174	116	1.23*	170	0.50	85.0	9.8	11.5	9.74	0.4	8.0
	These RF operating values were measured subsequent to failure and re-etch after that failure. *Measured at 88.0 Volts.											
P	1x3	AV174	84	-	166	0.90	149	19.2	12.9	9.1	1	20
	1x3	AV174	84	-	165	1.00	165	21.7	13.2	9.4	1	20
	One diode in the assembly failed when it was being operated at a reduced pulse width (0.75 μsec) but standard duty (20%).											
Q	1x3	AV174	102	1.38*	149	0.46	68.5	9.3	13.5	10.36	1	20
	One diode in assembly failed at low current (0.54 Amp). *C_T Measured at 80.0 Volts.											
R	1x3	AV174	104	-	154	0.71	109.3	14.6	13.3	9.17	1	20
	All three diodes failed when assembly dropped mode.											
S	1x2	AV174	64	-	92	0.60	55.2	6.7	12.1	9.72	1	20
	One diode failed when assembly dropped mode.											
T	1x2	AV174	58	-	Diode failed at low current (0.45 Amp) with no RF output.							
U	1x2	AV174	78	-	One diode failed at low current (~ 0.3 Amp), before RF output was achieved							
V	1x3	AV174	96	-	149	0.64	95.4	13.7	14.3	9.7	1	20

Table 2. RF Test Summary

After the initial three-chip assembly, efforts were concentrated on fabrication of two-chip assemblies. The next two assemblies were two-chip unpackaged assemblies - E failed at low current when the diamond lifted from the diode slug, while F achieved 19.7 w at 13.4% efficiency. Assembly G failed due to a coolant leak within the test fixture.

Assemblies H and I were also two-chip, unpackaged devices. H ran at 14.0 w output and 14.0% efficiency; I ran at 14.0 w with 18.4% efficiency. Both of these assemblies failed during the RF tests, and the leads were removed from H so that an SEM analysis could be performed. Figure 15 shows an edge burnout on the top chip on assembly H. It was suspected that assembly I failed due to the same mechanism, and the entire assembly was re-etched to an estimated 70% of its original size to clean up the surfaces of the chips. Assembly I was then retested and provided 16.0 w output at 14.3% efficiency.

Assemblies J and K were two-chip, unpackaged assemblies which provided an average 20.7 w output at an average efficiency of 15.6%. These two assemblies were shipped to General Dynamics on June 29, 1979.

Next, three two-chip assemblies were assembled in type AV174 ceramic packages obtained from Interceram. VSX9251AM-L and -M failed immediately at low current with no significant RF output. Assembly N achieved 15.4 w at 19.7% conversion efficiency.

Because of the inability to achieve reasonable output levels out of the two-chip assemblies, and in mutual agreement with General Dynamics, fabrication of three-chip packaged assemblies was begun. During the initial RF test, three-chip assembly O failed at low current when one diode developed an edge burnout. Figure 16 gives a closeup of the failure site.

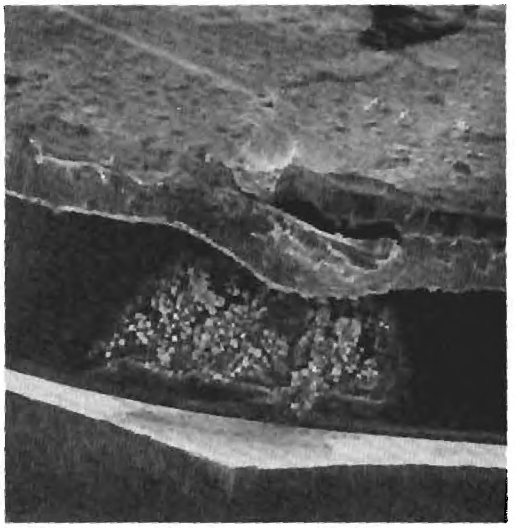


Figure 15. Two-Chip Assembly VSX9251AM-H. Mag. = 520X. Failed Diode Showing Edge Burnout.

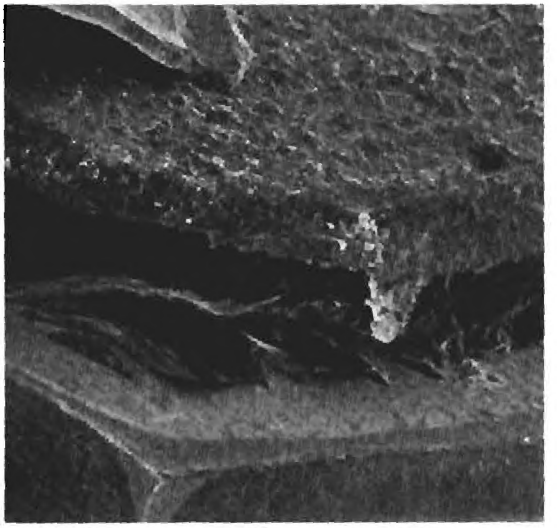


Figure 16. Three-Chip Assembly VSX9251AM-O. Mag. = 380X. Closeup of Failed Bottom Diode, chip # 43.

The diodes were etched to an estimated 50% of their original size, and the assembly provided 9.8 W output at 11.5% efficiency when operated at reduced pulse width and duty cycle. At this point the first batch of fifty chips had been exhausted of its diodes with good I-V characteristics, and the second batch of fifty was requested and received.

Assembly P was a three-chip packaged device using chips from the second batch of fifty. The assembly was tested at standard pulse width and duty with mediocre performance, then the device was tested at reduced duty and pulse width. The following data were taken.

VSX9251AM-P

[Watt] P_o	[%] η	[GHz] f_o	[μsec] P.W.	[%] Duty
19.2	12.9	9.1	1	20
21.7	13.2	9.4	1	15
20.7	10.4	9.6	1	10
15.1	11.9	9.3	0.75	20

The assembly failed during the 0.75 μsec pulse width test.

From these tests it appeared that the 1.0 μsec pulse width was satisfactory, but that 20% was not quite optimum. However, the overall poor performance of the assemblies cannot be attributed to nonoptimal pulse width. At this point the data taken on all of the RF tests were rechecked, it was seen that the RF operating current dropped from an average of 1.50 Amps for assemblies A-F, to 0.88 Amps for assemblies H-P. The thermal properties of the package were investigated and the results are presented in Section IV. In short, the effort was inconclusive—soldering a packaged assembly into the diode slug to improve heat flow did not enhance RF performance even though heat sinking was improved.

Six more multichip assemblies were fabricated—three with two chips and three with three chips. Of the two-chip assemblies, T and U failed at low current with no significant output; S managed 6.0 W out at 12.1% efficiency before failing. Assemblies Q and R averaged 12.0 W at 13.4% efficiency. Only assembly V survived testing, and produced 13.7 W at 14.3% efficiency.

Analyses to determine the cause of RF failure were done for a selected number of assemblies via the SEM. The results of the analyses for assemblies

H and Q have been presented as Figures 15 and 16. These two assemblies represent the two types of failures identified in the analyses. The first type, as illustrated by the photo for assembly H, is the surface burnout at the site of a geometrical defect in the mesa. Such a defect is often associated with contaminants, as mentioned previously in the discussion of the preselection data. A diode with surface burnout may be revived in many instances, if the surface is etched to remove the failed portion.

The second type of failure resulted from major cracks in the mesa. Assembly O exhibited this type of failure. An even more graphic example was presented by assembly U (see Figure 17). Although assembly O operated after being re-etched, diodes with major cracks cannot generally be revived. The assemblies which failed, and the reasons for their failure, if known, are outlined in Table 3.

In assemblies Q and T, a cracked diode was suspected as the cause of failure because dc characteristics which were free of premature breakdown before fabrication was begun became premature before RF testing was begun. The same type of degradation of the breakdown characteristics during fabrication was observed for assemblies S and U for which failure was known to be due to cracked devices. The cause of the cracks is not known, but is suspected to be excessive stylus pressure applied to the diodes either during preselection or in the bonding of leads to the back contacts during multichip fabrication.

Appendix 1 presents a more detailed summary of the disposition of the diodes and summarizes both the dc characteristics of the single chips and the RF operating characteristics of the completed assemblies. Four dc

Assembly	Type	Package	SEM?	Type or Cause of Failure
B	1x1	N-57	No	Unknown
D	1x3	No	No	Unknown
E	1x2	No	No	Mounting Diamond Lifted from Diode Slug
F	1x2	No	No	Unknown
G	1x2	No	No	Coolant Leak Within Test Fixture
H	1x2	No	Yes	Surface Burnout
I	1x2	No	No	Surface Burnout Suspected
L	1x2	AV174	No	Unknown
M	1x2	AV174	No	Unknown
N	1x2	AV174	No	Unknown
O	1x3	AV174	Yes	Cracked Diode
P	1x3	AV174	No	Unknown
Q	1x3	AV174	No	Cracked Diode Suspected
R	1x3	AV174	No	Unknown
S	1x2	AV174	Yes	Cracked Diode
T	1x2	AV174	No	Cracked Diode Suspected
U	1x2	AV174	Yes	Cracked Diode

Table 3. Failure Analysis Summary

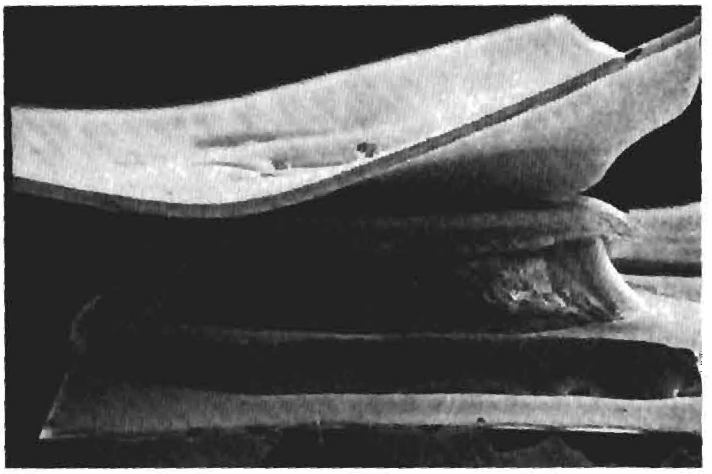


Figure 17. VSX9251AM-U Mag. 230X Cracked Diode Mesa in Multi-chip Assembly.

characteristics are included in the Appendix - premature breakdown, walkout, thermally induced hysteresis and slope parameter.

Premature breakdown usually results from a defect or localized non-uniformity in the semiconductor which causes that portion of the reverse biased diode to break into conduction at a lower voltage than the rest of the diode. Walkout is a measure of the difference in breakdown voltage at low and high currents. Thermal hysteresis describes the "ballooning" observed at high current. As the voltage is increased until the diode conducts a given current, the junction is heated. As the voltage is then decreased, the junction still remains heated, and the breakdown voltage associated with a given current is smaller in magnitude. Proper heat sinking of the diode will decrease the size of this thermally induced hysteresis.

The I-V curves for all one hundred chips were examined, and the amount of each of these three unwanted characteristics for each chip was labeled as slight (S), moderate (M), or excessive (E). Figures 18 and 19 illustrate the classification scheme for chips #1, 2, 19, and 20.

The fourth characteristic, slope parameter, is a merit figure of sorts, and was defined in conjunction with Figure 2. As the value of the parameter increases, the diode's merit decreases.

The data of Appendix 1 were investigated for a connection between dc characteristics and RF performance. The two-chip assembly which failed due to coolant leak (VSX9251AM-G) was excluded from the analysis. Also, the data from the two separate batches of fifty chips were looked at separately, and then the combined data for all chips were examined. For the first group of fifty, twenty-nine chips were used, fourteen of which failed under RF test. For the second group, eighteen diodes were used, eight of which failed.

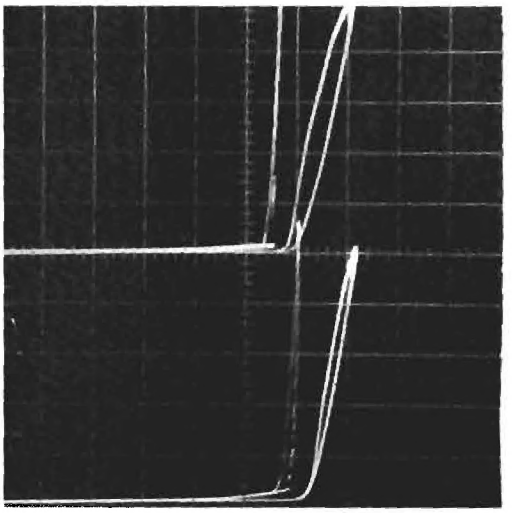


Figure 18. DC Characteristics, Chips 1 & 2

Vertical 1 = 0.2 mA/division
Vertical 2 = 10 mA/division
Horizontal = 5 V/division

	P.B.	W.O.	Balloon
Top (chip #2)	S	S	M
Bottom (chip #1)	M	S	S

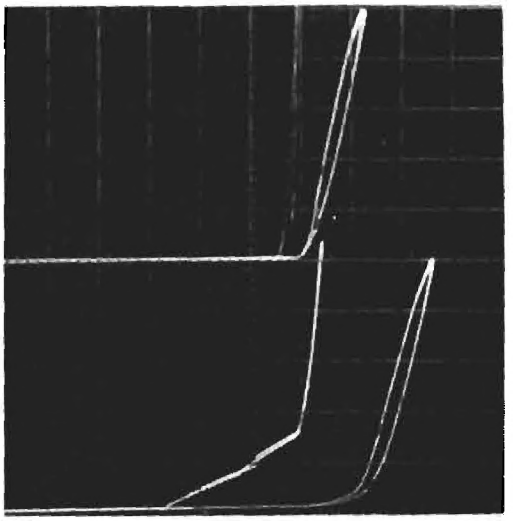


Figure 19. DC Characteristics, Chips 19 & 20

Vertical 1 = 0.2 mA/division
Vertical 2 = 10 mA/division
Horizontal = 5 V/division

	P.B.	W.O.	Balloon
Top (chip (#20)	S	S	S
Bottom (chip #19)	E	E	E

P.B. = Premature Breakdown
W.O. = Walkout
E = Excessive
M = Moderate
S = Slight

*Chip #19 data shown here was taken before etching and does not agree with data after etching the diode as recorded in Table 1.

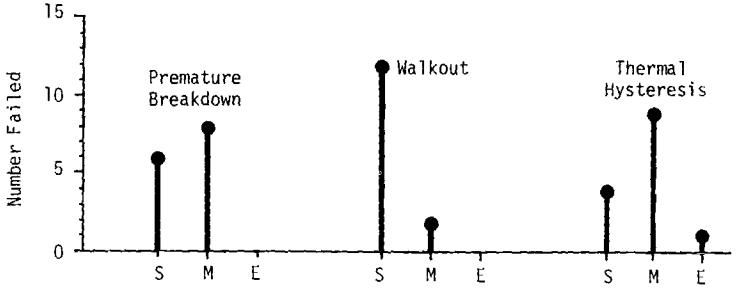
The histograms of Figures 20 through 25 plot the failed diodes and all diodes used on the multichips against dc characteristics measured in preselection. There appears to be no correlation between failure and slope parameter for either batch of fifty chips. Similarly, no correlation between the degree of walkout or thermally induced hysteresis of the chips and RF failure can be discerned.

However, the first batch of fifty chips (see Figure 20), diodes with moderate values of premature breakdown tended to fail more readily than those with slight. Of seventeen diodes with slight premature breakdown, only six failed (35%); of eleven used with moderate premature breakdown, eight failed (73%). For the second batch of fifty, there is no like correlation between premature breakdown and failure. The lack of correlation is probably due to the cracks in the mesa which appear to have dominated the failure mechanism. Otherwise, one would expect correlation between failure and premature breakdown for the second batch based on experience with the first batch of fifty.

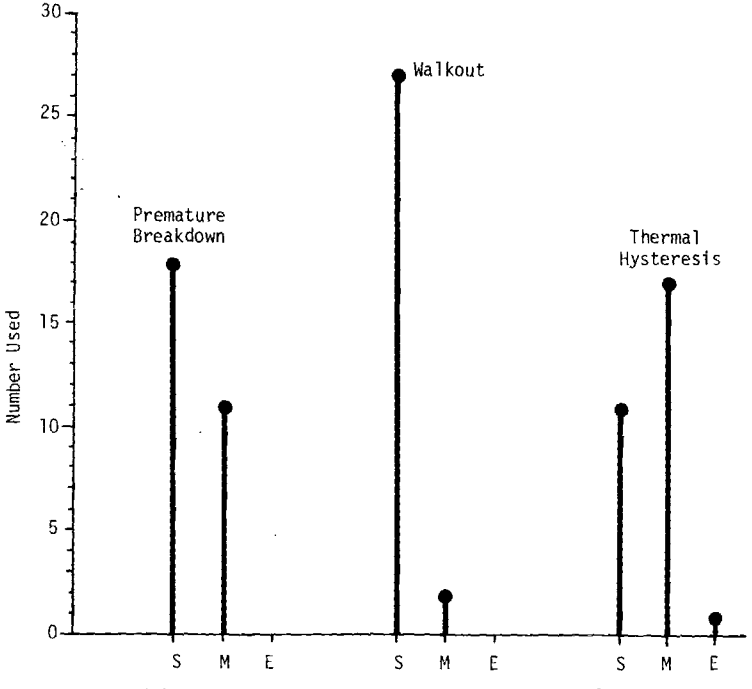
3.4 DELIVERIES

The following items have been delivered to General Dynamics in accordance with contract provisions.

Item	Delivery
(1) Nine Monthly Status Letters	Monthly, starting on 4/10/79
(2) Sketches of X-band Test Fixture	Included with Monthly Status Letter #3, sent on 6/14/79
(3) VSX9251AM-J and -K. Two unpackaged, two-chip assemblies	Shipped with cover letter on 6/29/79
(4) Final Report	2/18/80
(5) VSX9251AM-V. One packaged three-chip assembly	Shipped with Final Report

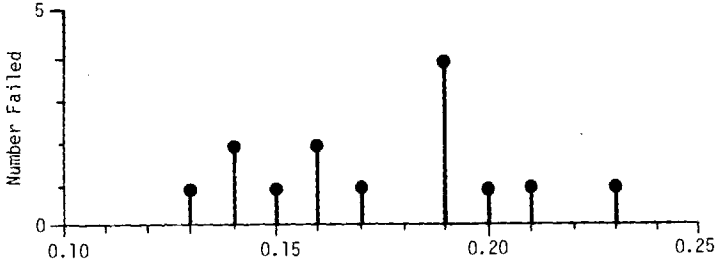


(a) Occurrence vs. DC Characteristics for Failed Chips

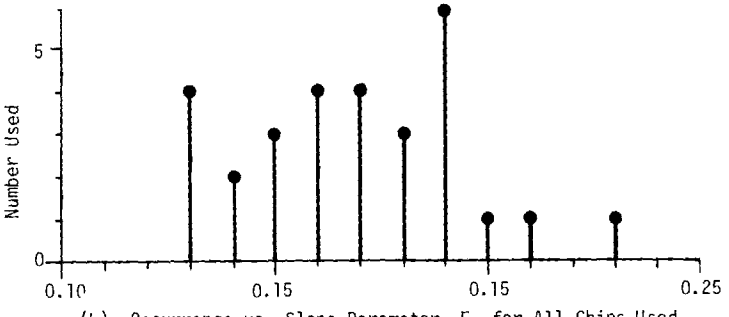


(b) Occurrence vs. DC Characteristics for All Chips Used

Figure 20. DC Characteristics Histogram for VSX9251AM, Chips 1-50.

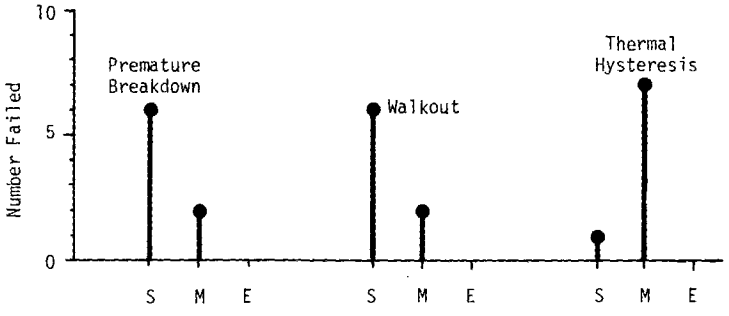


(a) Occurrence vs. Slope Parameter, F, for Failed Chips

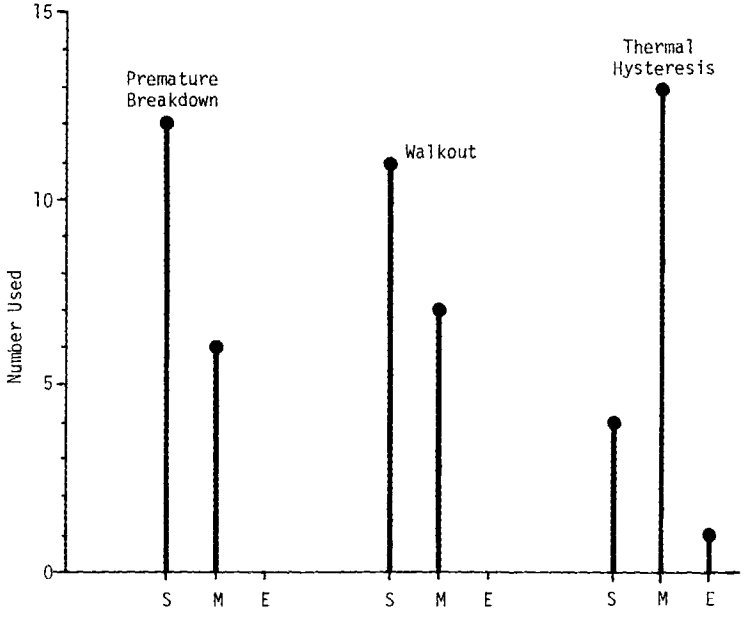


(b) Occurrence vs. Slope Parameter, F, for All Chips Used

Figure 21. Slope Parameter Histogram for VSX9251AM, Chips 1-50.

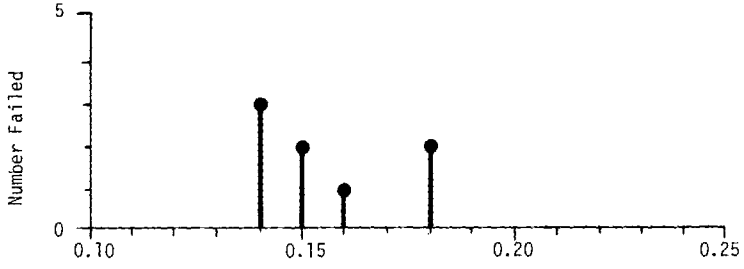


(a) Occurrence vs. DC Characteristics for Failed Chips

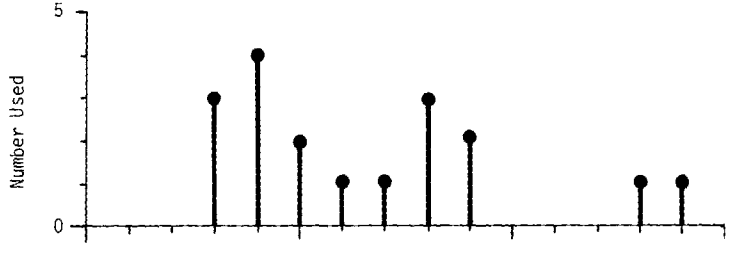


(b) Occurrence vs. DC Characteristics for All Chips Used

Figure 22. DC Characteristics Histogram for VSX9251AM, Chips 51-100

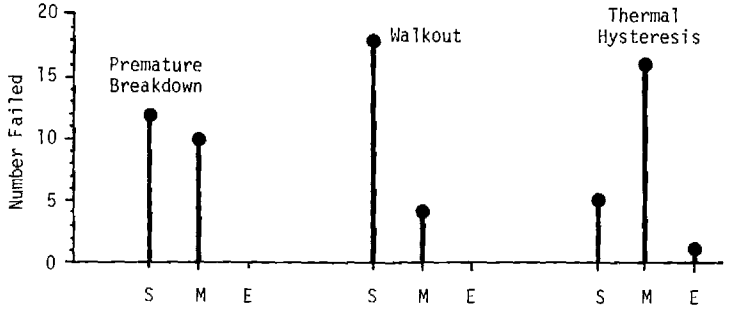


(a) Occurrence vs. Slope Parameter, F, for Failed Chips

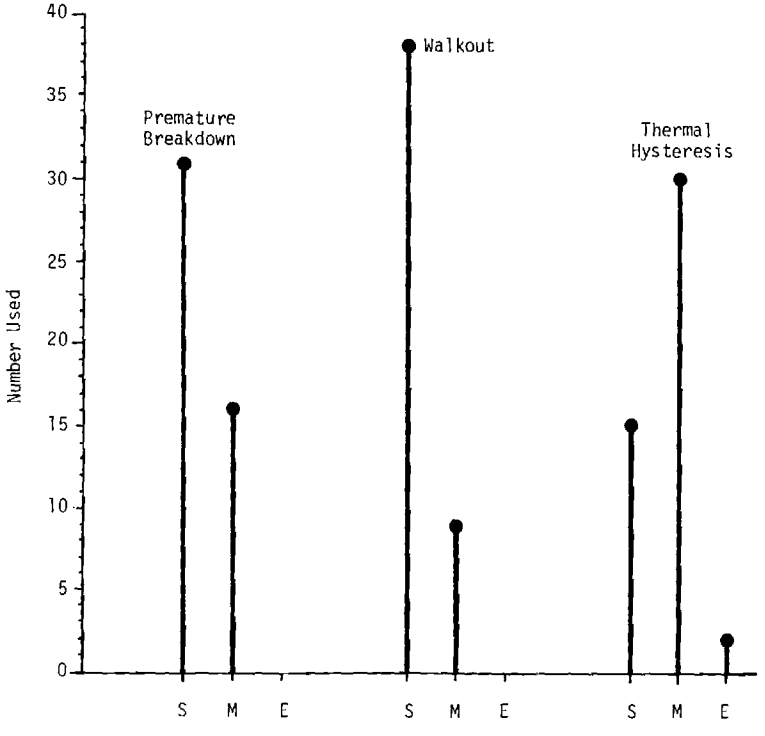


(b) Occurrence vs. Slope Parameter, F, for All Chips Used

Figure 23. Slope Parameter Histogram for VSX9251AM, Chips 51-100.

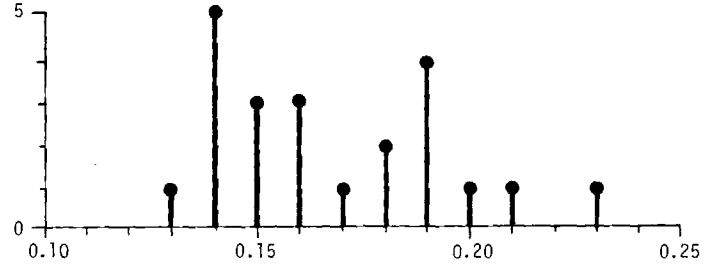


(a) Occurrence vs. DC Characteristics for Failed Chips

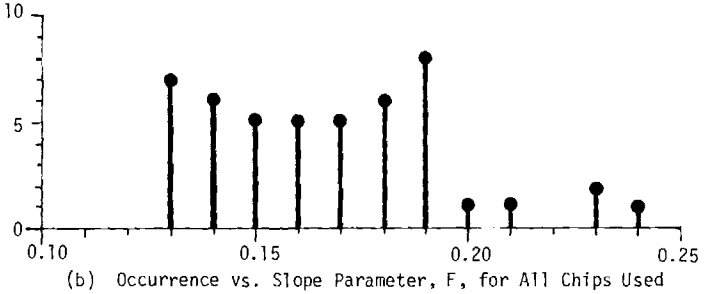


(b) Occurrence vs. DC Characteristics for All Chips Used

Figure 24. DC Characteristics Histogram for VSX9251AM, Chips 1-100.



(a) Occurrence vs. Slope Parameter, F, for Failed Chips



(b) Occurrence vs. Slope Parameter, F, for All Chips Used

Figure 25. Slope Parameter Histogram for VSX9251AM, Chips 1-100.

SECTION IV

THERMAL ANALYSIS

4.1 GENERAL

Table 4 presents a survey of the maximum operating currents obtained for the assemblies tested. Information for assemblies which never gave reasonable RF performance, but failed at extremely low output powers due to factors not related to current handling capabilities (e.g., failure due to a coolant leak) was left out of the table. Due to the large number of variables affecting RF performance, nothing conclusive could be inferred from the table, but it appears that there may have been overheating in the packaged multichip assemblies which limited the current capability when the packaged assemblies were screwed into the puck.

To investigate the possible heat dissipation problem, thermal measurements were made on a two-chip, packaged assembly with the assembly screwed into the one-half inch diameter slug (1) without heat sink grease, (2) with heat sink grease, and (3) soldered into the slug. The tests showed significant decrease in the thermal resistance from (1) to (2) to (3); however, enhanced RF performance was not attained with the device soldered into the diode slug.

4.2 MEASUREMENT TECHNIQUE

A detailed discussion of thermal resistance of an IMPATT is included as Appendix 2. To summarize this discussion, it can be shown that the thermal resistance of a diode is equivalent to the ratio of the change in junction temperature to the change in power dissipation resulting from raising the input current, $\theta_T = \Delta T_j / \Delta P_{diss} = \partial T_j / \partial P_{diss}$.

ASSEMBLY	TYPE	PACKAGE	I_{op}(max)	Duty
VSX9251AM-A	1x1	N-33	1.25 Amps	20.%
B	1x1	N-57	1.52	20.
C	1x1	N-57	1.55	20.
D	1x3	No	1.50	20.
"	1x3	No	1.60	10.
"	1x2	No	1.53	20.
F	1x2	No	1.52	20.
H	1x2	No	1.00	20.
I	1x2	No	1.00	20.
J	1x2	No	1.30	20.
K	1x2	No	1.30	20.
L	1x2	AV174	0.40	20.
M	1x2	AV174	0.25	20.
N	1x2	AV174	0.90	20.
O*	1x3	AV174	0.25	20.
"*	1x3	AV174	0.52	10.**
P	1x3	AV174	0.90	20.
"	1x3	AV174	1.00	15.
"	1x3	AV174	1.28	10.
Q	1x3	AV174	0.46	20.
R	1x3	AV174	0.71	20.
S	1x2	AV174	0.60	20.
T	1x2	AV174	0.45	20.
U	1x2	AV174	0.30	20.
V	1x3	AV174	0.64	20.

* This diode was etched to about 1/2 of its original area before it resumed operation after failure during the initial RF test.

** Pulse width - 0.3 μsec.

NOTE: These figures give the maximum operating currents obtained during the RF tests and are not necessarily the same as the currents listed in Table 2 which represent the operating conditions leading to maximum output power.

Table 4. RF Operating Current Summary.

Below 100 °C, IMPATT diodes typically exhibit a breakdown voltage, V_B, which is a linearly increasing function of junction temperature. If the diode is held at a constant temperature by an external heater and pulsed to a reference current level, I_{ref}, by a pulse narrow enough not to change the junction temperature ($\tau < 1$ μsec) the breakdown voltage may be recorded for that temperature. If this measurement is repeated for various values of T_j, the change in breakdown voltage is also seen to be a linear function of the change in junction temperature:

$$\Delta V_B = m_t \Delta T_j$$

where m_t is a constant slope parameter. Equivalently, we have $m_t = \partial V_B / \partial T_j$.

If dc bias power greater than I_{ref} is applied to the device, the breakdown voltage will increase. Again, using a narrow pulse, the current may be momentarily returned to the value I_{ref}. Upon repeating the process at increasingly higher values of DC bias current, the change in breakdown voltage measured at I_{ref} is a linear function of the power dissipated in the device at the higher value of bias current:

$$\Delta V_B = m_p \Delta P_{diss}$$

$$\text{or } m_p = \partial V_B / \partial P_{diss}$$

But from the definition of thermal resistance,

$$\theta_T = \partial T_j / \partial P_{diss} = \frac{\partial V_B / \partial P_{diss}}{\partial V_B / \partial T_j}$$

Thus thermal resistance can be readily determined to be

$$\theta_T = m_p/m_t$$

4.3 THERMAL MEASUREMENT RESULTS

Thermal measurements were made on two assemblies which had survived previous RF testing. The data taken for both assemblies appear in Appendix 3. VSX9251AM-A was a single chip assembly mounted in a type N-33 micropill package. Heat sink grease was applied to the threads, and the package screwed into the puck. A thermal resistance of θ_T = 17.2 °C/watt was observed for the device.

Measurements were then made on the two-chip assembly, VSX9251AM-N, with the assembly screwed into the slug (1) with heat sink grease, (2) without heat sink grease and (3) soldered into the slug. The results are summarized as follows:

Assembly VSX9251AM-N

THERMAL MEASUREMENTS

Mounting to Puck	[V/°C] m_T	[V/watt] m_p	[°C/watt] θ_T
Without Heat Sink Grease	0.232	2.52	10.90
With Heat Sink Grease	0.232	1.67	7.20
Soldered	0.241	1.41	5.85

The assembly showed a decrease in θ_T of almost one-half ($\frac{10.9-5.85}{10.9}$ = 0.46) when progressing from an assembly simply screwed into the slug without grease to the same assembly soldered into the slug, a surprisingly large change. The reduction in thermal resistance suggested that improved RF

performance might be forthcoming for the assembly soldered into the slug. The assembly was RF tested and the data compared with previous data for the same diode mounted in the slug with only heat sink grease.

RF Performance VSX9251AM-N

Mounted With Heat Sink Grease: 9/4/79

[volts] V	[Amps] I	[watts] P	[watts] P_o	[%] η	[GHz] f_o	[μsec] P.W.	[%] Duty
105.	0.80	84.0	16.7	19.9	9.7	1	20

Soldered Into Diode Slug: 11/19/79

106.	0.90	95.4	13.7	14.3	9.7	1	20
100.	0.80	80.0	10.4	13.0	10.0	1	15
95.	0.70	66.5	7.5	11.3	10.2	1	10

The diode did not behave as expected. With decreased thermal resistance, higher efficiency and power output were expected from the soldered device. When poorer performance was observed at 20% duty cycle, the duty was dropped to 15%, then 10%, with even poorer results. The poorer results may have been due to possible damage suffered by the diodes when they were soldered into the package. In retrospect, it is also possible that the dramatic decrease in thermal resistance may have been partially due to imperfections in the threaded slug. Although the assembly was screwed in tightly, the threads at the extreme surface of the slug in use were enlarged during constant use, and the fit between the shoulder of the package and

slug may not have been as snug as it should have been for the trials with and without heat sink grease. When the assembly was soldered into the slug, the gaps, if indeed they existed, were filled with solder so that the problem was eliminated. Additional tests to verify the large change appeared to be in order. Unfortunately, the project schedule and funding did not allow for additional measurements.

SECTION V

CONCLUSIONS AND RECOMMENDATIONS

5.1 CONCLUSIONS

The single chips supplied by the vendor, Varian Lot No. VSX9251AM: 1-100, were only capable of producing reduced outputs and efficiencies when assembled and tested at Georgia Tech. The RF output, at best, was on the order of 10-11 W at 15% efficiency. Power outputs of two and three times those available from one chip were successfully demonstrated from unpackaged assemblies containing two and three chips, respectively. The same was not achieved for the multichip assemblies in AV174 packages, however. Neither the two nor the three-chip assemblies were able to produce the power expected. Although the thermal tests were inconclusive, a problem may exist with AV174 packages when they are not soldered into their mounts. Inadequate heat sinking is the prime suspect in explaining the inability of the packaged multichips to attain the expected levels of power output. With diode chips having improved quality and power, it is strongly felt that two and three-chip assemblies in AV174 packages capable of producing two and three times the output of a single chip, respectively, are practical devices.

Failure analysis revealed that multichips assembled from the first batch of fifty diodes did not survive RF testing primarily due to the failure of chips which had shown moderate to excessive levels of premature breakdown during preselection. Failures of multichips assembled from the last batch of fifty chips appeared to be due to cracks in the mesa of some of the diodes. These cracks were probably caused either by the preselection process or by improper bonding stylus pressure applied during the

fabrication of the assemblies. If the cracks had not been present, it is felt that failure would have again primarily been due to unacceptable levels of premature breakdown associated with many of the chips.

The results of the failure analysis are in agreement with observations from previous chip combining work—diodes with premature breakdown fail under stress more readily than those with sharp breakdown. All of which reinforces the feeling that with higher quality chips and proper heat sinking, two and three-chip packaged assemblies are feasible.

5.2 RECOMMENDATIONS

Further thermal tests are needed to determine the heat sinking requirements of multichip assemblies mounted in type AV174 packages. Such tests should be conducted with assemblies using higher quality chips than those available for this program. In particular, chips capable of higher power output (on the order of 15-20 W), and possessing improved breakdown characteristics are needed. Packaged multichips are almost certain to be attainable; they should be considered for use in circuit type power combining circuits to be incorporated in developmental systems.

APPENDIX 1

DIODE CHIP CHARACTERISTICS AND DISPOSITION

DIODE LOT VSX 9251AM

GENERAL DYNAMICS

Summary 8/16/79

Chip No.	dc Characteristics				Use			Op. Status		Comments
	P.B.	W.O.	T.H.	F	Con.	Dsg.	Pkg.	Chip	Assy	
1	M	S	S	0.135	1x1	B	N-57	No	No	Assy. dropped mode.
2	S	S	M	.171	1x1	A	N-33	Yes	Yes	RF performance satisfactory
3	S	S	S	.131	1x1	C	N-57	Yes	Yes	Low RF efficiency
4	M	M	M	.190	1x2	L	AV174	No	No	Assy. failed at 0.4 Amp
5	M	S	S	.154	1x2	H	No	No	No	Assy. failed at 1.0 Amp
6	S	M	M	.140	1x3	D	No	No	No	Assy. converted to 1x2
7	M	M	M	.212						Unused
8	S	S	M	.198	1x3	O	AV174	No	No	Assy. failed at 0.5 Amp
9	M	S	S	.130	1x2	H	No	No	No	Assy. failed at 1.0 Amp
10	S	S	M	.178	1x2	K	No	Yes	Yes	Delivered to General Dynamics
11	S	S	M	.186	1x2	L	AV174	Yes	No	Assy. failed at 0.4 Amp, No RF
12	M	S	M	.190	1x2	M	AV174	No	No	Assy. failed at 0.25 Amp
13	M	M	E	.245						Unused
14	M	S	M	.211	1x2	N	AV174	No	No	Failed during thermal experiment
15	S	S	M	.171	1x2	I	No	Yes	Yes	Assy. operational after re-etch
16	S	S	S	.150	1x3	D	No	Yes	No	Assy. converted to 1x2
17	M	S	S	.162	1x2	N	AV174	No	No	Failed during thermal experiment
18	M	E	E	.259						Unused
19	S	E	E	.323						Unused
20	S	S	S	.165	1x2	E	No	Yes	No	Assy. failed at 0.6 Amp
21	E	M	E	.211						Unused

Chip No.	dc Characteristics				Use			Op. Status		Comments
	P.B.	W.O.	T.H.	F	Con.	Dsg	Pkg.	Chip	Assy	
22	S	S	M	.161	1x2	E	No	No	No	Assy. failed at 0.6 Amp.
23	S	S	S	.131	1x2	J	No	Yes	Yes	Delivered to General Dynamics
24	S	S	M	.180	1x2	M	AV174	Yes	No	Assy. failed at 0.25 Amp.
25	M	E	M	.237						Unused
26										Chip failed during preselection
27	M	M	M	.170						Unused
28	S	S	M	.186	1x2	K	No	Yes	Yes	Delivered to General Dynamics
29	M	S	E	.226	1x2	F	No	No	No	Assy. failed at 1.5 Amp.
30	S	S	M	.190	1x3	O	AV174	No	No	Assy. failed at 0.5 Amp
31										Chip failed during preselection
32	S	S	M	.161	1x2	I	No	Yes	Yes	Assy. operational after re-etch
33	M	S	E	.209						Unused
34	M	M	M	.175						Unused
35	M	S	S	.154	1x2	F	No	Yes	No	Assy. failed at 1.5 Amp
36	S	S	M	.226						Chip destroyed during fabrication
37	M	S	S	.128	1x2	G	No	Yes	No	Assy. failed due to coolant leak
38	M	S	S	.156	1x2	J	No	Yes	Yes	Delivered to General Dynamics
39	E	M	M	.170						Unused
40	S	M	E	.131						Unused
41	M	E	M	.185						Unused
42	M	E	M	.188						Unused
43	S	S	M	.171	1x3	O	AV174	No	No	Assy. failed at 0.5 Amp
44	S	S	E	.292						Unused
45	M	S	M	.151						Unused
46										Chip failed during preselection

Chip No.	dc Characteristics				Use			Op. Status		Comments
	P.B.	W.O.	T.H.	F	Con.	Dsg.	Pkg.	Chip	Assy.	
47	S	S	M	.177	1x3	D	No	Yes	No	Assy. converted to 1x2
48	S	S	M	.187	1x2	G	No	No	No	Assy. failed due to coolant leak
49	S	S	S	.173						Unused
50	M	S	M	.194						Unused
51	M	M	S	0.147						Developed severe premature breakdown when etched
52	M	M	M	0.186	1x2	U	AV174	Yes	No	Assy. failed at 0.3 Amp, no RF
53	E	M	M	0.230						Unused
54	E	M	M	0.186						Unused
55	S	S	M	0.198						Unused
56										Chip failed during preselection
57	S	S	S	0.129	1x2	S	AV174	Yes	No	Assy. failed at 0.64 Amp, mode drop
58	M	M	M	0.256						Unused
59										Chip failed during preselection
60	S	S	E	0.229	1x3	V	AV174	Yes	Yes	Low operating current, RF output
61	M	M	M	0.178	1x2	U	AV174	No	No	Assy. failed at 0.3 Amp, no RF
62	S	M	M	0.238	1x3	V	AV174	Yes	Yes	Low operating current, RF output
63	M	S	M	0.162						Unused
64	M	E	M	0.217						Unused
65	M	M	M	0.186						Unused
66	E	M	M	0.166						Unused
67	E	S	S	0.135	1x3	P	AV174	No	No	Assy. failed at 0.85 Amp, mode drop
68	M	S	M	0.167	1x2	T	AV174	Yes	No	Assy. failed at 0.45 Amp, no RF
69	S	S	M	0.168						Unused
70	S	S	M	0.154	1x2	T	AV174	No	No	Assy. failed at 0.45 Amp, no RF

Chip No.	dc Characteristics				Use			Op. Status		Comments
	P.B.	W.O	T.H.	F	Con.	Dsg.	Pkg.	Chip	Assy.	
71	M	M	M	0.133	1x3	V	AV174	Yes	Yes	Low operating current, RF output
72	S	S	M	0.138	1x3	R	AV174	No	No	Assy. failed at 0.75 Amp, mode drop
73	S	E	S	0.152						Developed severe premature breakdown when etched
74	S	S	M	0.158	1x2	S	AV174	No	No	Assy. failed at 0.64 Amp, mode drop
75	S	S	M	0.186						Developed severe premature breakdown when etched
76	S	S	M	0.179	1x3	Q	AV174	No	No	Assy. failed at 0.54 Amp, mode drop
77	M	E	S	0.188						Unused
78	M	S	M	0.156						Unused
79	M	M	M	0.175	1x3	Q	AV174	Yes	No	Assy. failed at 0.54 Amp, mode drop
80										Lost during shipping
81	S	S	M	0.154	1x3	R	AV174	No	No	Assy. failed at 0.75 Amp, mode drop
82	S	S	S	0.142	1x3	P	AV174	Yes	No	Assy. failed at 0.85 Amp, mode drop
83	S	M	M	0.140	1x3	R	AV174	No	No	Assy. failed at 0.75 Amp, mode drop
84	M	E	M	0.177						Unused
85	S	S	M	0.175						Developed severe premature breakdown when etched
86	M	S	M	0.142						Unused
87	M	S	S	0.156						Unused
88	S	S	S	0.129	1x3	P	AV174	Yes	No	Assy. failed at 0.85 Amp, mode drop
89										Chip failed during preselection
90	E	M	M	0.186						Unused
91	S	S	M	0.178						Unused
92	S	S	M	0.171						Unused
93	M	S	M	0.160						Developed severe premature breakdown when etched

Chip No.	dc Characteristics				Use			Op. Status		Comments
	P.B.	W.O.	T.H.	F	Con.	Dsg.	Pkg.	Chip	Assy.	
94										Chip failed during preselection
95										Chip failed during preselection
96	M	M	M	0.165						Unused
97	M	M	M	0.167						Unused
98	E	S	M	0.146						Unused
99	E	M	M	0.178						Unused
100	S	M	M	0.189	1x3	Q	AV174	Yes	No	Assy. failed at 0.54 Amp, mode drop

Legend: P.B. = Premature Breakdown
W.O. = Walkout
T.H. = Thermally Induced Hysteresis
F = Slope Parameter
Con. = Configuration
Dsg. = Designation, e.g. "A" means the chip was used in assembly VSX9251AM-A
Assy. = Assembly
Op. Status - Operational Status, i.e., is the chip (or assembly) still working?
E = Excessive
M = Moderate
S = Slight

APPENDIX 2

DETAILED DISCUSSION OF THE MEASUREMENT OF THERMAL RESISTANCE

A. Theory

The total thermal resistance of a diode, θ_T, is the ratio of temperature change to dc power dissipated in the diode. If the temperature reference is that of the diode slug (heat sink) into which the packaged diode is screwed, then θ_T includes the junction to package thermal resistance and the package-to-heat sink thermal resistance. This may be expressed as

$$\theta_T = \frac{T_j - T_s}{P_{diss}} \qquad (1)$$

where T_j = junction temperature,

T_s = heat sink temperature and

P_{diss} = power dissipated.

The most straightforward way to measure θ_T would be to apply known power to the diode, and measure T_j and T_s directly with thermocouples and/or infrared radiometers. This method is impractical for most purposes, however.

A more convenient method relies on the fact that the breakdown voltage, V_B, is a function of the junction temperature. Over the range of measurement interest (20 °C to 100 °C), the dependence is approximately linear with temperature. At higher temperatures, V_B is not usually a linear function of temperature. Therefore, a single unique thermal resistance value is not determinable. For the purpose of comparing thermal resistances between diodes, the maximum of 100 °C is sufficient.

Figure 1 gives the I-V characteristics of a reverse biased IMPATT diode. The curves labeled "ISOTHERMAL" are those obtained at different

ambient temperatures when the test voltage and current pulses are so short compared to the thermal time constant of the diode, that the pulse does not change the junction temperature. A pulse width of less than 1 μsec is typically required. The curve labeled "DC" adds the effect of the increase in breakdown voltage with temperature to the isothermal curves. It may be obtained by increasing the current from a dc supply to the diode in increments and taking the data point-by-point.

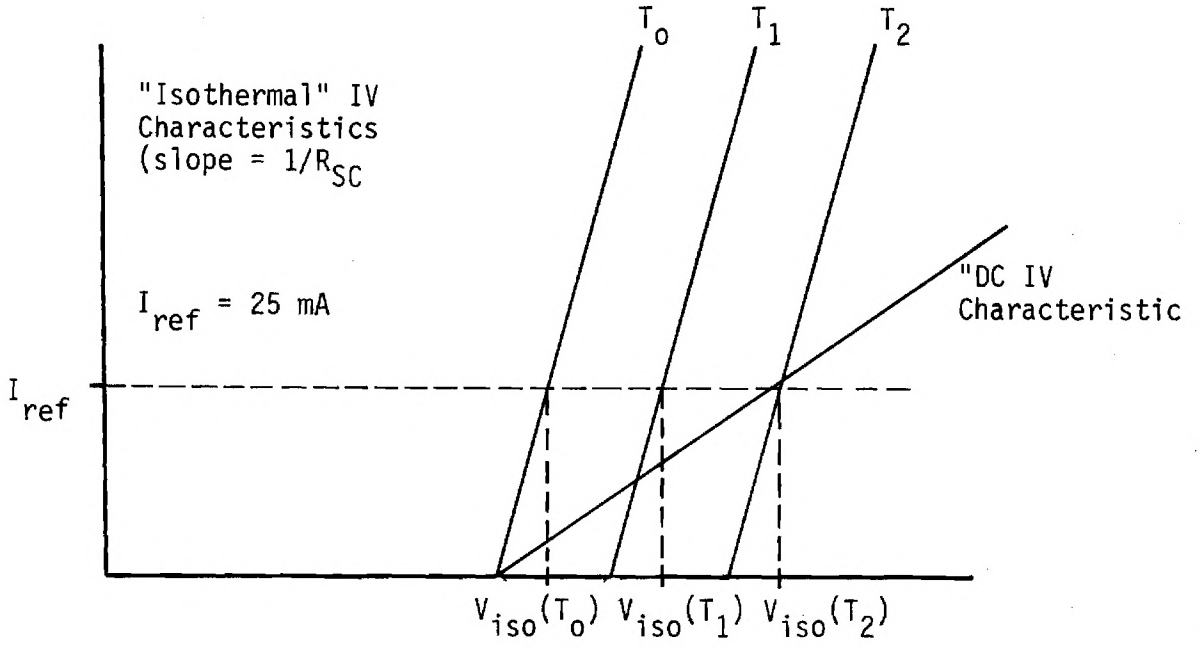


Figure 1. I-V Characteristics of Reverse Biased IMPATT Diode

The voltage across the diode may be expressed as a function of the junction temperature (T_j) and current (I) in the following manner:

$$V(T_j,I) = V_B(T_j) + I\ R_{SC},$$

where R_{SC} = space charge resistance measured in the absence of thermal effects.

Expansion of $V_B(T_j)$ about T_o yields

$$V_B(T_j) = V_B(T_o) + \frac{\partial V_B}{\partial T}\Big|_{T_o} [T_j - T_o] + \cdots$$

or $$V_B(T_j) \cong V_B(T_o) + \beta\, V_B(T_o)\, [T_j - T_o]$$

where $$\beta = \frac{1}{V_B(T_o)} \frac{\partial V_B}{\partial T}\Big|_{T_o} .$$

The total voltage may then be expressed as

$$V(T_j,I) = V_B(T_o) + \beta\, V_B(T_o)\, [T_j - T_o] + I\, R_{SC} .$$

The power dissipated in the diode is given by

$$P_{diss} = I\, V(T_j,I) = I\, V_B(T_o) + I\, \beta\, V_B(T_o)\, [T_j - T_o] + I^2\, R_{SC}$$

or $$T_j - T_o = \frac{V(T_j,I) - V_B(T_o) - I\, R_{SC}}{\beta\, V_B(T_o)} .$$

Applying the definition of equation (1), one has:

$$\theta_T = \frac{V(T_j,I) - V_B(T_o) - I\, R_{SC}}{I\, \beta\, V(T_j,I)\, V_B(T_o)} . \qquad (2)$$

By directly measuring R_{SC} and β, which is an effective voltage-temperature calibration, one may obtain the thermal resistance. Early efforts took this direct appoach[1,2]. The measurement procedure described below uses the method with slight modifications to ease computation of θ_T.

B. Measurement Procedure

Figure 2 shows the apparatus used to make thermal measurements. The dc power supply must be capable of supplying up to 150 mA of current at breakdown. The heater is a resistor anchored to a copper plat of approximate dimensions 2-1/2" x 2" x 3/16" which also has water cooling provisions. The packaged diodes were screwed into a threaded diode slug which was then clamped to the plate. A thermocouple was installed in the slug near the package. Pulse length and duty were set at 0.3 μsec and 0.05%, respectively, and maintained at those values for all measurements.

Step A of the measurement was a voltage temperature calibration. Water flow established both the heat sink (diode slug) and diode junction temperature at some initial reference temperature, T_o, after which coolant flow was stopped. Throughout Step A, the dc supply was adjusted to provide 1 mA bias current to maintain the device near breakdown. By superposition, it may be shown that the dc supply and pulser wavefore combine to produce a composite waveform as shown in Figure 3. The pulser was set to provide a pulse level, I_{ref} = 25 mA.

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1. R.H. Haitz, et al., "A Method for Heat Flow Resistance Measurements in Avalanche Diodes," IEEE Trans. Electron Devices, vol. ED-16, No. 5, pp. 438-444 May 1969.

2. "Pulse Measurements of Transient Thermal Response and Temperature of Avalanching p-n Junction," Electronics Letters, vol. 7, no. 17, p. 481., 26 August 1971.

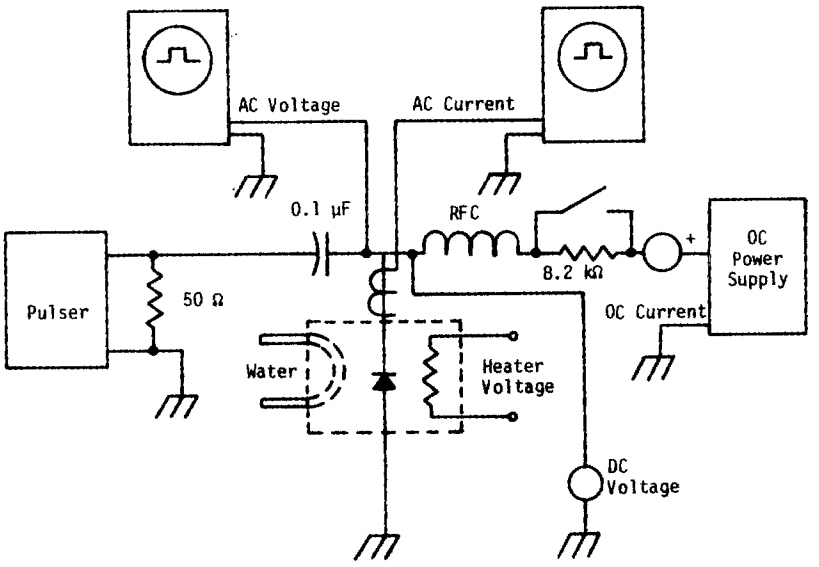
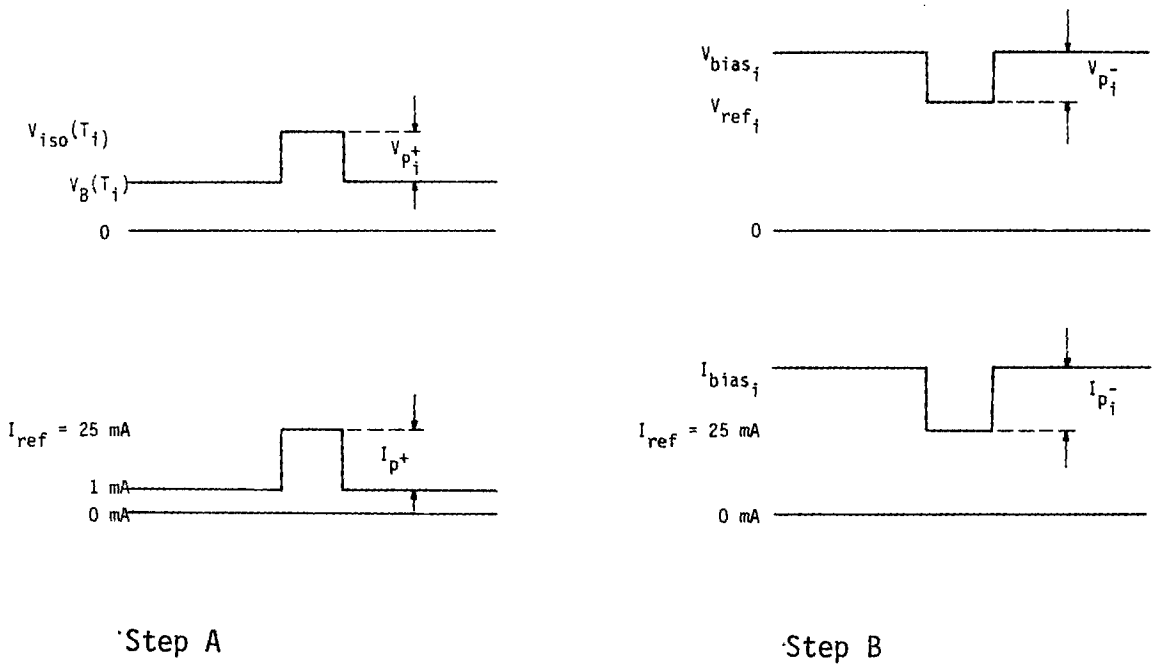


Figure 2. Thermal Resistance Measurement Block Diagram



Step A

Step B

Figure 3. Thermal Measurement Voltage and Current Waveforms

The voltage increase, $V^{+}_{P_o}$, due to the current pulse when added to the bias voltage, $V_B(T_o)$ yielded the "isothermal" voltage corresponding to a 25 mA current level. Call this voltage $V_{iso}(T_o, 25\ mA)$. Next, the temperature was raised to T_1 by the auxiliary heater, then $V_{iso}(T_1, 25\ mA)$ was measured. This procedure was repeated to obtain $V_{iso}(T_i, 25\ mA)$ for several higher temperatures, T_i. When the voltage is plotted against temperature, one obtains the incremental change of the breakdown voltage, V_B, with temperature:

$$m_t \triangleq \frac{\Delta V_B}{\Delta T_A} = \frac{V_B(T_i) - V_B(T_o)}{T_i - T_o} = \frac{V_{iso}(T_i, 25\ mA) - V_{iso}(T_o, 25\ mA)}{T_i - T_o}$$

where i = temperature index.

Note that m_t is constant for $T_i < 100\ °C$ because of the linear dependence of V_B on junction temperature.

In step B, the dependence of breakdown voltage on power dissipation was first obtained, then converted to the dependence of temperature difference on power which determined θ_T. The dc bias current was first set to 25 mA = I_{bias_o}, and the water used to set the heat sink temperature at T_{S_o}. Because of the high bias, the junction temperature was elevated to a temperature T_{j_o}, such that $T_{j_o} > T_{S_o}$. The dissipation, $P_{diss_o}(25\ mA)$ and dc voltage V_{ref_o} were then measured at the 25 mA level.

The bias current was increased to higher levels $I_{bias_1}, \ldots, I_{bias_i}, \ldots$, for which there were higher power dissipations $P_{diss_1}, \ldots, P_{diss_i}, \ldots$ At these higher bias levels, a negative going current pulse was used to return the current to I_{bias_o} along an isothermal characteristic. Figure 4 illustrates the quantities involved in Step B. The magnitude of the voltage

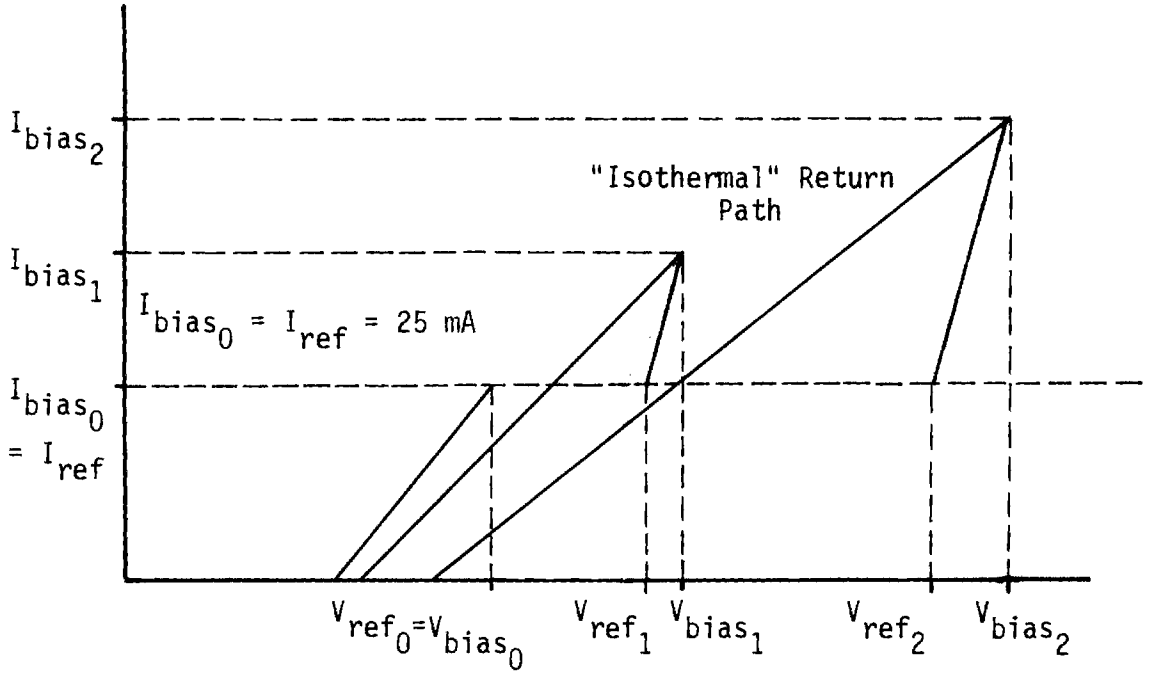


Figure 4. Operating Conditions for Step B of Thermal Resistance Measurement

pulses corresponding to these current pulses was denoted by $\bar{V}_{P_i}$. The voltages $V_{ref_i} \triangleq V_{bias_i} - V_{P_i}$, are the voltages of the T_{j_i} isothermal evaluated at a current level of $I_{bias_o} = 25$ mA. The difference in these voltages, $\Delta V_{ref_i} \triangleq V_{ref_i} = V_{ref_o}$, corresponded to the difference of the two junction temperatures. The junction temperature difference was calculated via the calibration of Step A.

$$\Delta T_{j_i} = T_{j_i} - T_{j_o} = \Delta V_{ref_i} \left(\frac{\Delta T_A}{\Delta V_B}\right)$$

Recall the definition of thermal resistance:

$$T_j - T_s = \theta_T \cdot P_{diss}$$

$$(T_{j_i} - T_{s_i}) - (T_{j_o} - T_{s_o}) = \theta_T(P_{diss_i} - P_{diss_o})$$

If the sink is held constant $T_{s_i} = T_{s_o}$, and

$$\theta_T = \frac{T_{j_i} - T_{j_1}}{P_{diss_i} - P_{diss_o}} = \frac{\Delta T_{j_i}}{\Delta P_{diss}} \quad .$$

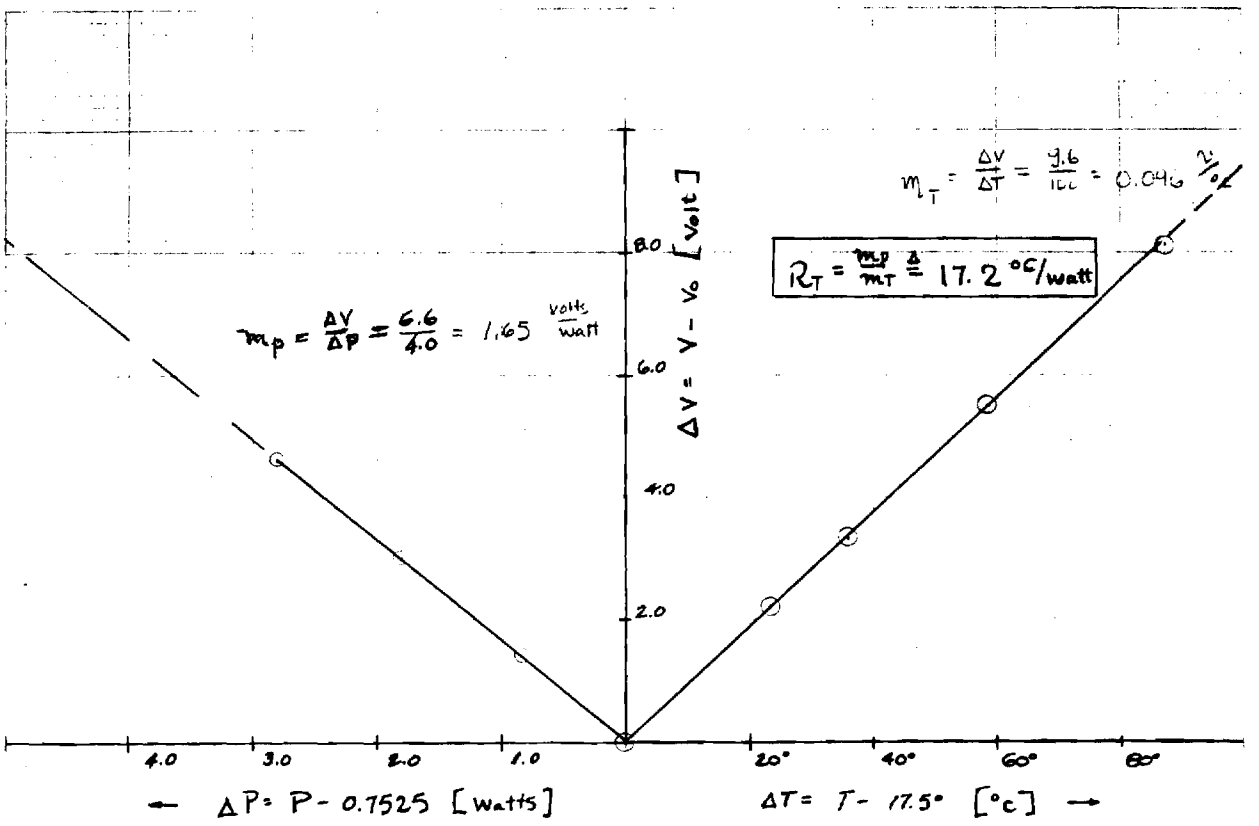
If we define $m_p = \frac{\Delta V_{ref_i}}{\Delta P_{diss_i}}$, and note that m_p is a constant then

$$\theta_T = \frac{m_p}{m_t} \tag{3}$$

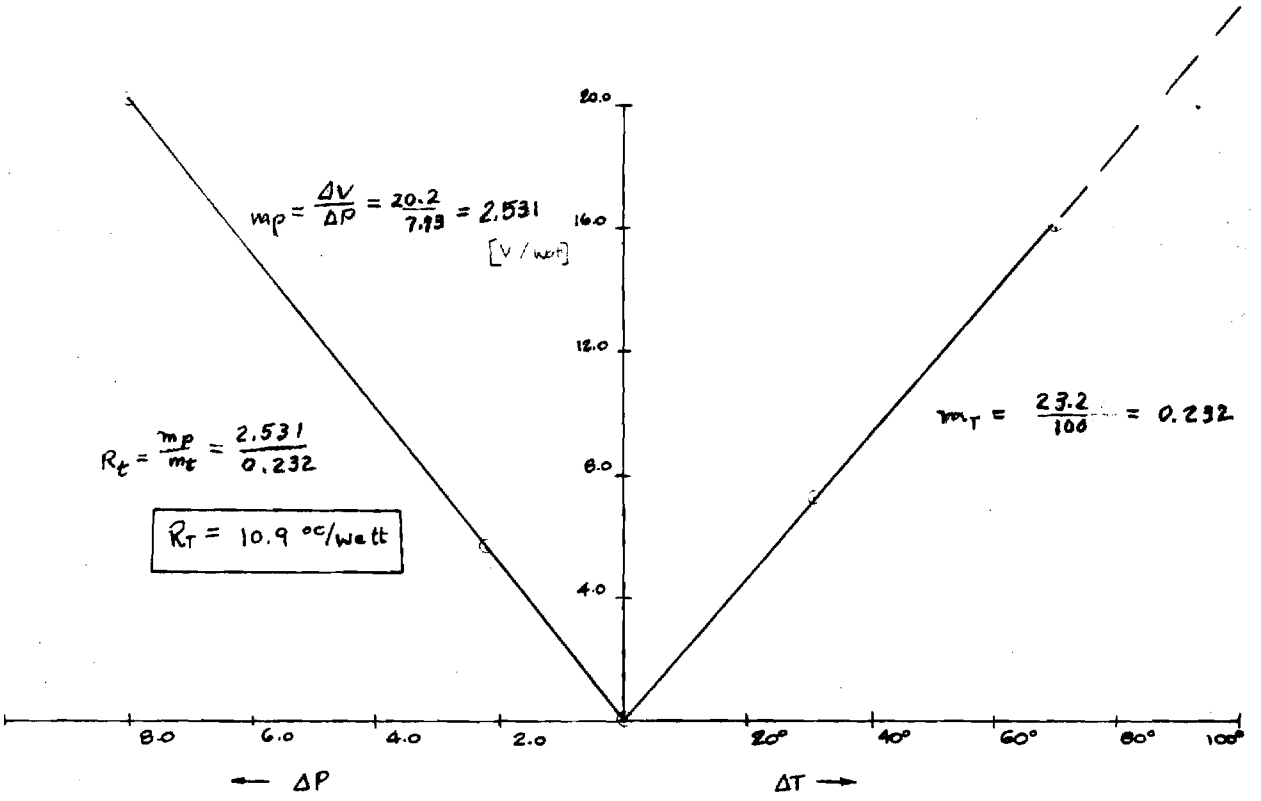
Equation (3) gives thermal resistance in terms of the quantities actually measured and plotted. Calculation of R_{SC} and β is possible from the data taken, but not necessary.

APPENDIX 3

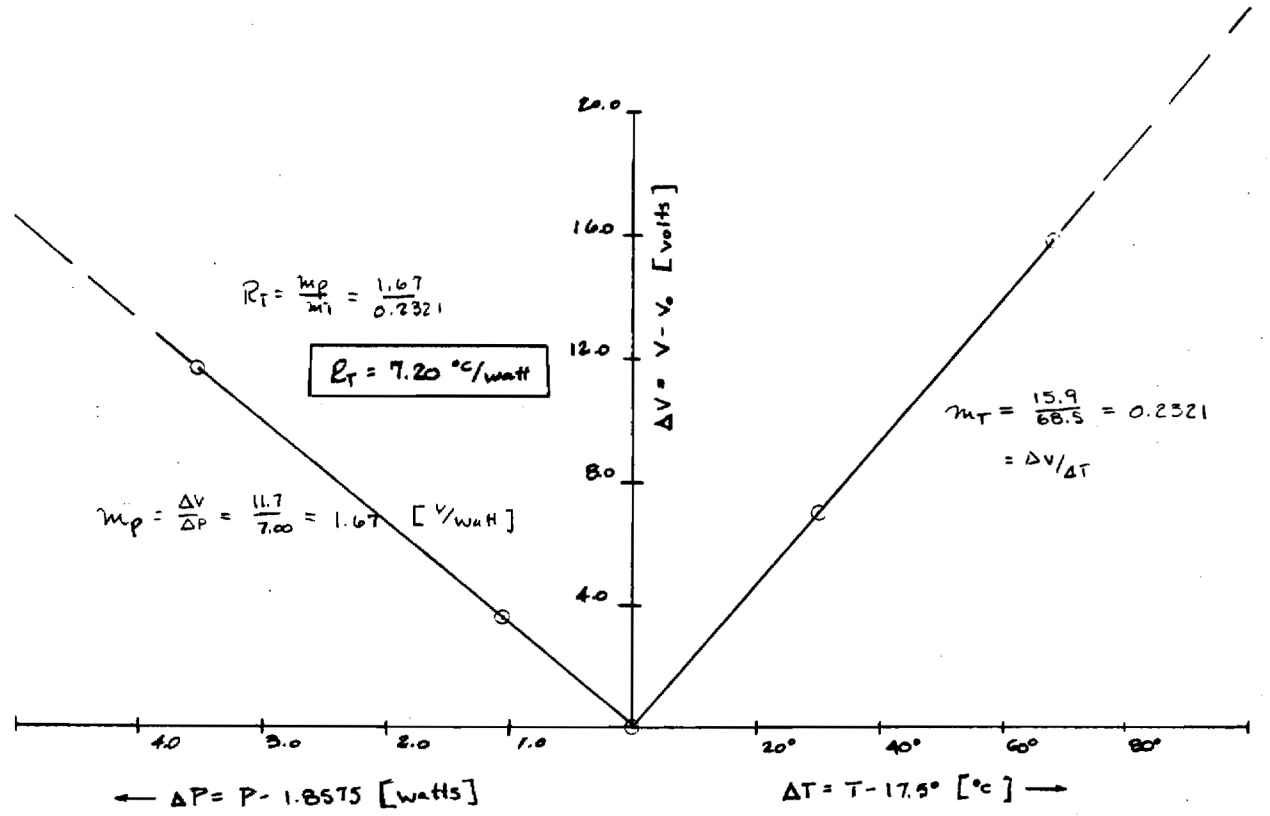
THERMAL RESISTANCE MEASUREMENT DATA



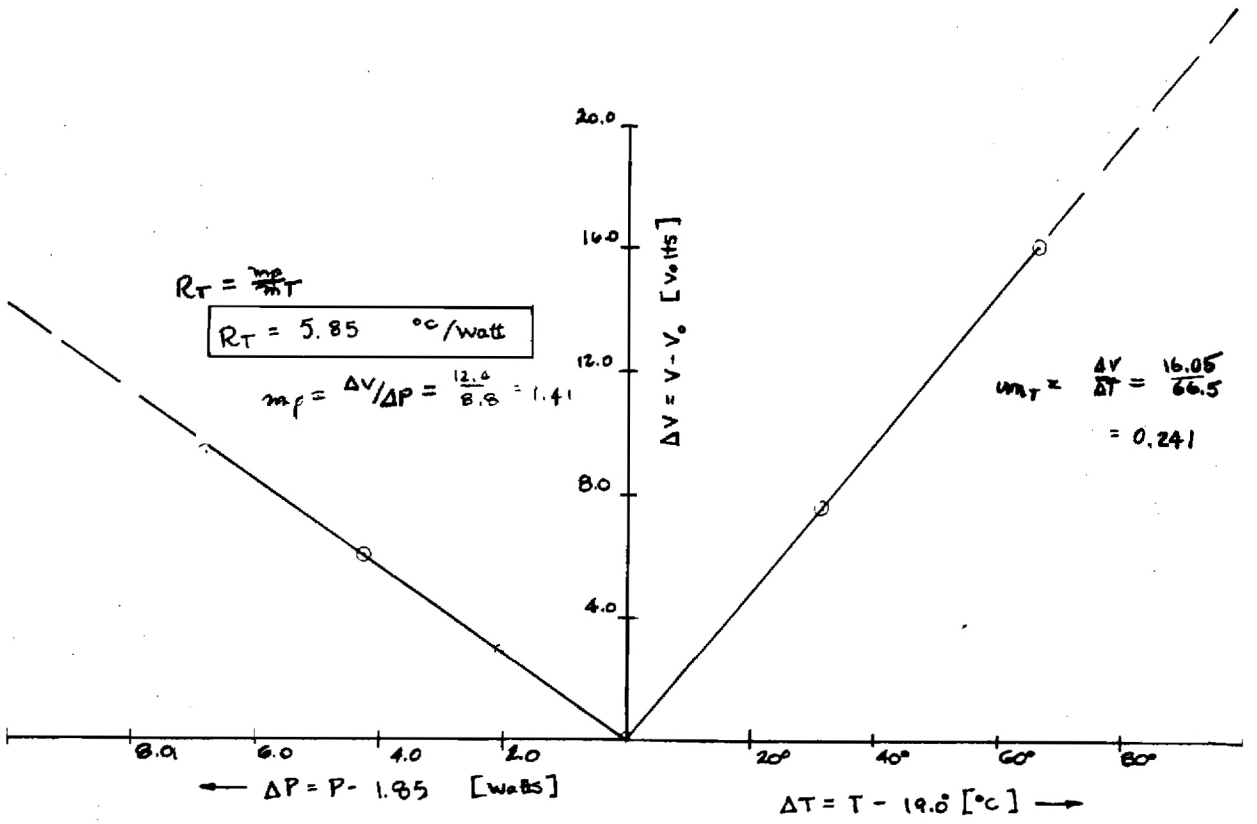
Thermal Measurement: 11/8/79
VSX9251AM-A (N-33, 1x1)



Thermal Measurement: 11/13/79
VSX9251AM-N (AV174, 1x2)
W/O Heat Sink Grease



Thermal Measurement: 11/12/79
VSX9251AM-N (AV174, 1x2)
With Heat Sink Grease



Thermal Measurement: 11/15/79
VSX9251AM-N (AV174, 1x2)
Assembly Soldered into Diode Slug